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Low Power Two-Stage Operational Amplifier design using 45 nm Technology

Navneet Dubey
Research Scholar
ITM University,
Gwalior (M.P.) [INDIA]
Email: navneet.dubey8@gmail.com

Dr. Shyam Akashe
Professor
Department of Electronics and Communication Engg.
ITM University
Gwalior (M.P.) [INDIA]
Email: shyam.akashe@itmuniversity.ac.in

Abstract**—***For low power Circuit work at the low voltage supply, but at low voltage supply voltage integrated circuitry design start to face a power wall as the most difficult constrains. In new technology and large demand in market of portable electronics equipment are increasing the interest in very low power integrated circuits. Designing very low power integrated circuit requires the reduction of the internal power supply voltages and interconnection parasitic element should be at least less and as these are the most important parameters that had been associated to power dissipation at certain supply to maintain the circuit performance at low voltage supply reduced the threshold voltage of the transistor which impose a large number of serious problem caused in both in circuit design and applied technology and techniques. After decreasing the threshold voltage the margin for error problems decrease and operational amplifier circuit parameter dramatically degrade the performance of original circuit thus in this paper we used current compensation technique to minimize the certain power consumption of low power amplifiers.*

Keywords:**—***AC analysis, DC analysis, Transient analysis gain, Power dissipation, Cadence.*

1. INTRODUCTION

Operational amplifier, which has become new of the most versatile and important building blocks in analog circuit design. There are two operational amplifier developed. Operational Trans conductance amplifiers (unbuffered) have the output resistance typically very high. The other one is the buffered amplifier (voltage operational amplifier) typically low output resistance. Operational amplifier (control source) that have high forward gain so that when negative feedback is applied, the closed loop transfer function is practically independent of the gain of operational amplifier. This principal has been exploited to develop many useful analog circuit and system. The primary requirement of an operational amplifier is to have an open loop gain that is sufficiently large to implement the negative feedback concept. Here we use current compensation technique to minimize the power consumption here we design the operational amplifier using cadence 180nm technology and 65nm technology and calculate the gain and power consumption.

There are many factors that are diving the need to have lower power supply voltages in CMOS integrated circuits. As the channel length of CMOS technology decrease, the maximum allowable voltage will decrease. Also, as more components are include in the same area on integrated circuit, the power

dissipation increase. Finally, the requirement for portable electronics implies battery operation which favour low voltage and low power circuits. These factors and other have caused many to suggest that future implementation of mixed analog digital circuit using standard CMOS will have power supplies more than 1v or less an important factor concerning analog circuits is that threshold voltage of future standard

CMOS technologies are not anticipated to decrease much below what is available today. It is necessary that the analog power supply be at least equal to the sum of the magnitude of the n-channel and p-channel threshold. This implies that low voltages analog circuits are in compatible with the CMOS technology trends of the future. Ways to circumvent this conflict are to develop technologies with lower threshold, increase the lower voltage power supply by on-chip dc-dc converter, or develop circuit techniques that are compatible with future standard CMOS technology trends.

The basic operational amplifier consists of four main blocks which as follows:

A. Dual input Differential output.

B. Differential input single ended output.

C. Level shifter.

D. Output buffer.

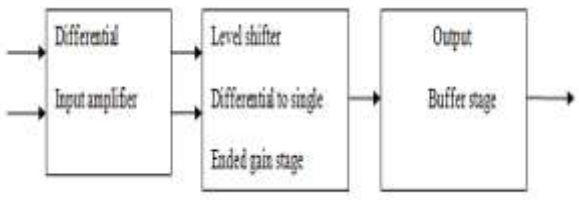

Figure1: The general structure of operational amplifier

Complementary metal oxide semiconductor operational amplifier is very similar in architecture to their bipolar counter parts and also having an improvement in processing had been pushed scaling of device dimension persistently over the past many years. The main drive behind this trend is the resulting reduction in production cost since more components on a chip are possible. In addition to device scaling, the increase in the portable electronics market is also encouraging low voltage and low power circuitry since this would reduce battery size and weight and enable longer battery life time.

The third approach, developing analog circuit's techniques that compatible with future CMOS technology. There are many important advantage of certain approach thus; firstly, the need to develop expensive CMOS technology with less threshold voltages is avoided than Secondly, the high efficiency dc to dc converters are not even required. Thirdly, circuit techniques that permit low voltages operation with large threshold offer the potential for more fully utilizing the technology at higher voltages and at lower voltages if, might also be an fact the low threshold technologies do become standard technologies to be in use.

2. OP-AMP PRACTICAL CONSIDERATIONS

2. 1. Input/Output Offset Voltage

Op-amps do not always perform practically as they should theoretically. For example, sometimes an output voltage exists when both inputs are grounded. This output voltage is called output offset voltage and it is caused by an input offset voltage. If one is known the other can be calculated,

$$Vio = V_{oo} / A_v$$

Imperfect transistors contained in the differential amplifier are responsible for the input offset voltage, which is usually no more than 2mV. The offset null pins on the IC op-amp can be used with a potentiometer to take care of Vio and Voo.

2. 2. Input Bias Current / Input Offset Current

Similar to the offset voltages, there are currents flowing in or out of the inputs, and

their average is known as input bias current, which may have a value of 80nA+. The currents on each input are not always equal and the difference between them is the input offset current. This is important because if the input bias currents are different, then the output voltage can be affected. So to keep the currents the same, each input needs to see the same resistance to ground, since identical currents will flow through identical resistances.

2. 3. Common Mode Rejection Ratio (CMRR)

The common mode rejection ratio (CMRR) is a ratio of the normal high gain that amplifies the difference of the signals on the inputs to the undesirable gain that amplifies a value when the signals are the same

CMRR = Adiff/Acm

If op-amps were perfect, then there would be zero amplification when the same signal, or common-mode signal, feeds each input. The common-mode signal may be noise, so obviously it is not a good thing to amplify this noise. An acceptable CMRR is in the 90's (dB), where

CMRR = 20 log (Adiff/Acm) {in decibels (dB)}

2. 4. Output Short-Circuit Current

Op-amps do not output unlimited current because too much current flow could be damaging to the op-amp, particularly if a short circuit develops. Op-amps are made this way on purpose. An output short-circuit current of 25mA is a common value for an op amp. It follows that a low resistance load does not drop the expected voltage.

3. IMPLEMENTATION

Here we implemented the operational amplifier using current compensation technique in cadence technology. Figure shows below the schematics diagram of operational amplifier.

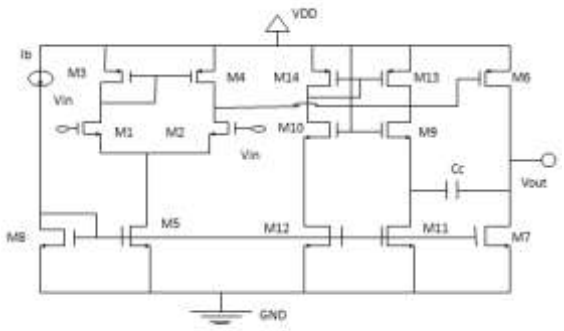

Figure 3 schematic diagram of op-amp

Figure shows below the schematic diagram of operation amplifier. Here we implemented the operational amplifier. In the following figure we use NMOS and PMOS transistor and with a capacitor c_c thus NMOS transistor consist of following transistors as M1, M2, M5, M8, M7, M9, M10, M11 and M12 and also PMOS transistors consist of M3, M4, M6, M13 and M14 to demonstrate feasibility of the proposed low power operational amplifier circuit.

Simulation:

The result of the different analysis in cadence technology is listed below in tabular form. The cut off frequency at different voltages is shown in table1 and operating at supply voltage of 1.5v. Different parameter of the OP-AMP and comparison between simulated result and previous paper result had been discussed as shown in figure 2 and figure 3 were calculated at cadence technology.

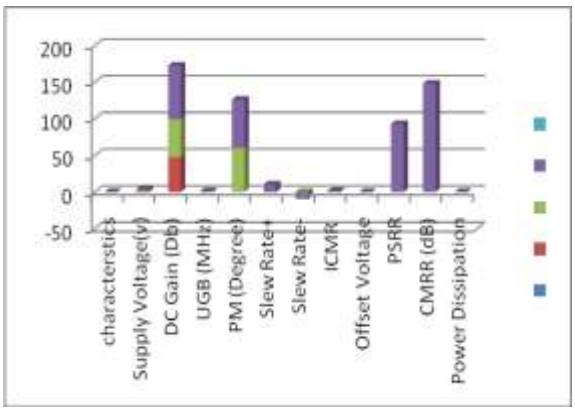

Figure 2: Comparison between simulated results and previous paper

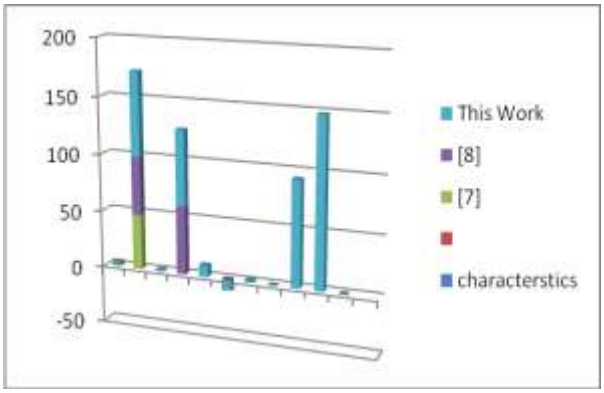

Figure 3: Comparison between Previous paper and proposed work.

From the following figure 2: we had a comparisons between various simulated results of low power operational amplifiers and also for previous results which consists of supply voltage, characteristics, dc gain, UGB, PM, slew rate, ICMR (Input/output common mode range), offset voltage, PSRR (Power supply rejection ratio), CMRR (Common mode rejection ratio) along with power is being calculated with the simulated graph as shown above

Characte-ristics	[2]	[3]	[4]	[5]	[7]	[8]	This Work
Supply Voltage(V)	3	1.5	1.5	2	1.5	0.8	1.5
DCGain (dB)	20.88	80	82	102	48	51	73.57
UGB (MH_Z)	15.4	167	1.15	0.48	NA	0.057	1.084
PM (Degree)	-19.6	73.5	86	60.35	NA	60	65.89
Slew Rate+	NA	464	0.73	0.20	NA	0.14	10.1
Slew Rate -	NA	NA	0.73	0.21	NA	NA	-9.5
ICMR	NA	1.13	NA	1.13	NA	NA	1.51
Offset Voltage	50	NA	NA	0.25	NA	NA	NA
PSRR	NA	NA	NA	59.7	NA	NA	92.95
CMRR (dB)	-53	NA	NA	102.004	NA	NA	147.9
Power Dissipation	570 (µw)	8.9 (mw)	NA	25.745 (mw)	6.5 (mw)	1.2 (µw)	3.54 (µw)

The main performance of our proposed operational amplifier are summarized in table 1; as shown the proposed operational amplifier achieve good performance characteristics in terms of DC Gain, Slew rate, and power dissipation which is as shown above.

4. CONCLUSION

This paper presents a new low power operational amplifier circuits operating with the supply voltages 1.5v and power dissipation is 3.54(µw). Proposed circuit can be used for wide verities of low voltages and low power application. The following paper shows simulated result having presented to demonstrate the feasibility of the proposed low power operational amplifier circuit. Cadence is used to verify the circuit performance. However in this paper we used compensation technique to minimize power consumption for maintain the circuit performance at low voltage supply reduced the threshold voltage of the transistor which impose a large number of serious problem both in circuit design and technology.

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