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Design and Implementation of Single Bit ALU Using PTL & GDI Technique

Nidhi Dubey
M.Tech. Research Scholar
Shri Ram Institute of Technology
Jabalpur (M.P.), [INDIA]
Email: niidhi.dubey25@gmail.com

Divyanshu Rao
Assistant Professor
Department of Electronics & Comm. Engineering
Shri Ram Institute of Technology
Jabalpur (M.P.), [INDIA]
Email: divyanshu3@gmail.com

Abstract**—***In this paper, the design of a one bit ALU using Pass Transistor Logic combined with Gate Diffusion Input technique is being done which is implemented using minimum transistor full adder and also adapts hardware reuse method which has advantages of minimum transistors requirement, more switching speed and low power consumption with respect to the conventional CMOS techniques Single Bit ALU is being implemented with PTL & GDI technique in DSCH 3.5 and layout generated in Microwind tool. The Simulation is done using 65 nm technology at 1.2 v supply voltage and result is compared with conventional CMOS technique. Simulation result shows great improvement in terms of area, switching delay and power dissipation.*

Keywords:—*GDI, PTL, CMOS, Switching Delay, Power dissipation*

1. INTRODUCTION

The ALU is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. The processors found inside modern CPUs and Graphics Processing Units (GPUs) have inside them very powerful ALUs. The power consumed by the ALU has a direct impact in the power dissipated from the processor. Hence, a design is required to implement the ALU in a fashion where the performance of the processor is improved and also the power consumed is less. Power consumption of whole data path can be reduced by reducing power consumption of ALU. Adder is the basic building block for an ALU. To reduce the power consumption from ALU first we need to reduce through full adder. We have designed ALU by using multiplexer and full adder circuit. The pass transistor design reduces the parasitic capacitances and results in fast circuits. The multiplexers have been used in the ALU design for input and output signals selection. The multiplexer is implemented using pass transistors. This design is simple and efficient in terms of area and timing.

The full adder performs the computing function of the ALU and can be implemented in two types of logic structures, namely static style and dynamic style. Static full adders are commonly more reliable, simpler and lower power than dynamic ones. However, dynamic full adders are faster and sometimes more compact than static full adders. However, dynamic full adders suffer from charge sharing high power due to high switching activity, clock load and complexity. Full adder is an essential component for designing all types of processors viz. digital signal processors (DSP), microprocessors etc.

In the present work, the design of a one bit Arithmetic And Logic Unit (ALU) using

Pass Transistor and Gate diffusion input technique and Full Adder block is presented and results are compared with that of conventional ALU using CMOS technique and CMOS Full Adder block. The functionality and performance is analyzed using Microwind Software tool. Since Microwind integrates front-end and back-end design into an integrated flow, improving the design cycle and minimizing design complexities. It firmly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification. Performance parameters like area, power dissipation and propagation delay for both the ALU's are analyzed at 65 nm using 6metal layer CMOS technology and Microwind Software tool.

2. IMPLEMENTATION OF ADDER USING CMOS TECHNIQUE

Full Adder is the one of the basic element in Digital Circuits. It is also one of the critical building blocks of the ALU. We can deduce the Boolean function in SOP form for full adder as the following:

Here A and B are the inputs to the adder, C is the input carry, SUM is the output for add operation, and CARRY is the output for any carry generated. The generate signal, G, is high only when a carry output (CARRY) is internally triggered within the adder. When the propagate signal, P, is high, the carry-in signal C is passed on to the carry output CARRY. Because the Carry-in status of the current bit is obtained by lower of two operand bits, the delay of the adder therefore depends on the carry generation.

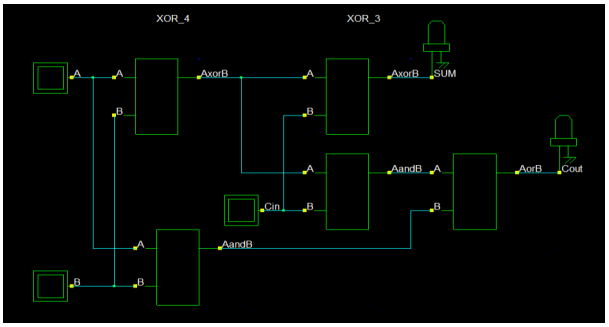

Figure 1 CMOS Full Adder Using Gates

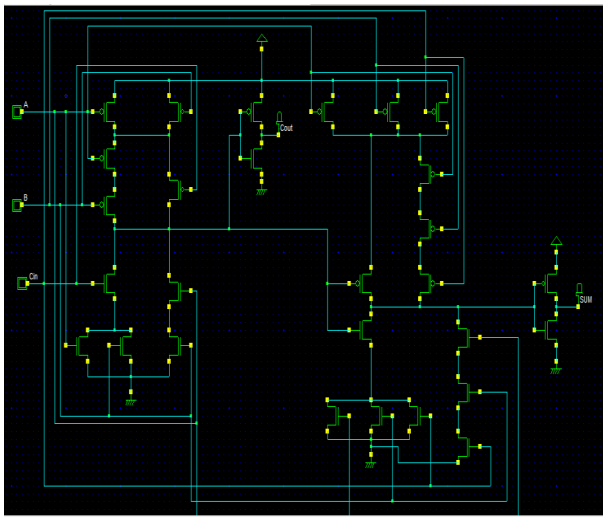

Figure 2 CMOS Full Adder Using 28 Transistors

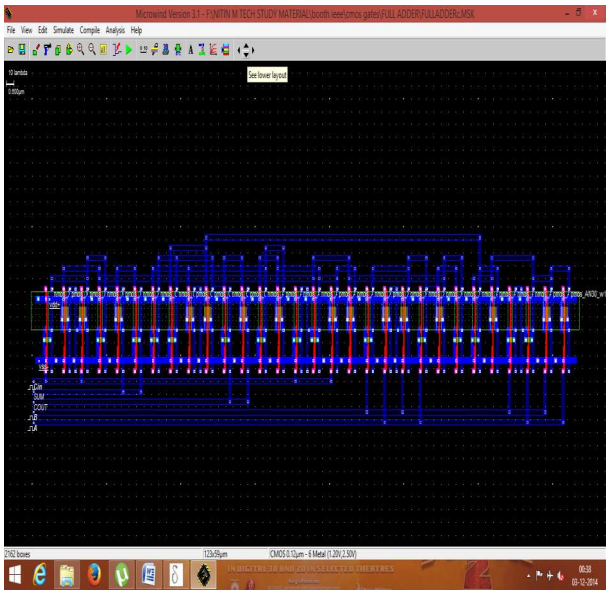

Figure 3 Layout of CMOS Full Adder Using Gates

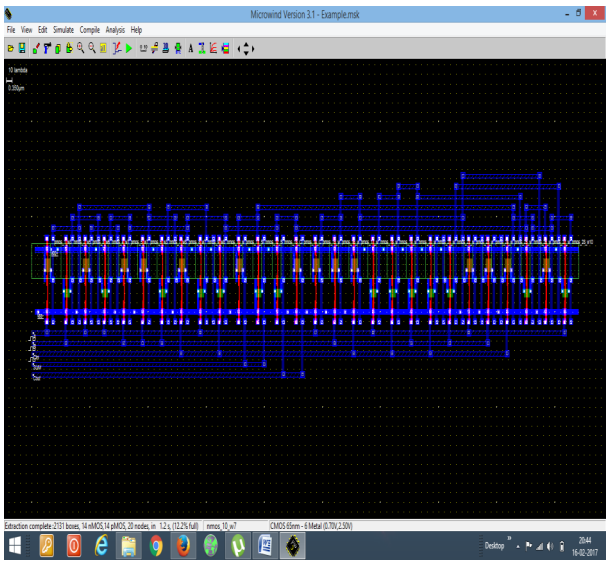

Figure 4 Layout of CMOS Full Adder Using 28 Transistors

3. IMPLEMENTATION OF ALU USING CMOS TECHNIQUE

After designing basic gates required for full adder and using these gates for adder implementation. It is observed from full adder logical equation that different logical operations can be derived from it. Logical equation of full adder is given by:

It is seen from full adder implementation that XOR & AND operation can be derived from full adder. So we only need an additional OR Gate only for design of ALU. Therefore final implementation of Single Bit ALU using CMOS technique is shown in figure

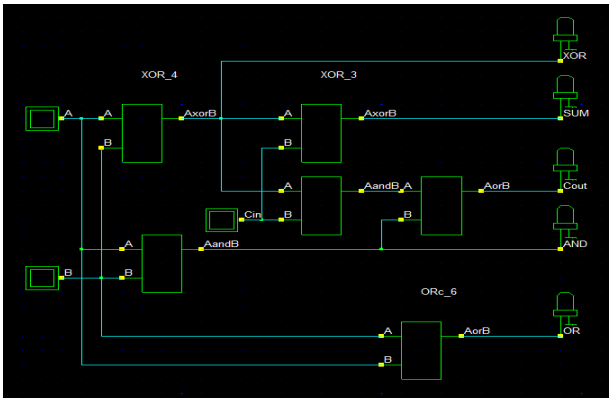

Figure 5 Single Bit ALU using CMOS Technique

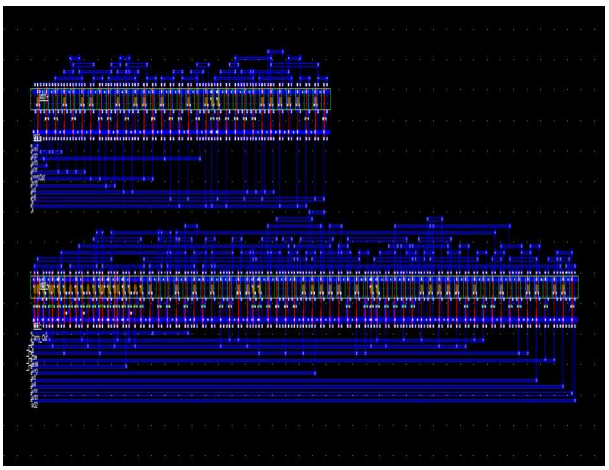

Figure 6 Layout of Single Bit ALU using CMOS Technique

4. IMPLEMENTATION OF ADDER USING PTL AND GDI TECHNIQUE

Full Adder can also be implemented using combined technique (GDI & PTL). This Full Adder design can also be reconfigured to be used as AND, OR, XOR and INVERTER gate along with addition operation. The modified equations for Full adder for this purpose are as follows:

$$sum = (a \oplus b) \oplus c$$
$$=> (a \oplus b)c`+(a \oplus b)`c$$
$$carry = ab + bc + ca$$
$$=> (a \oplus b)`a + (a \oplus b)c$$

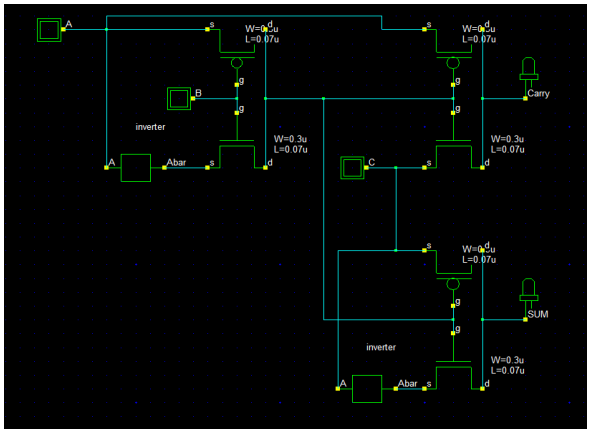

Figure 7 PTL & GDI Based Adder

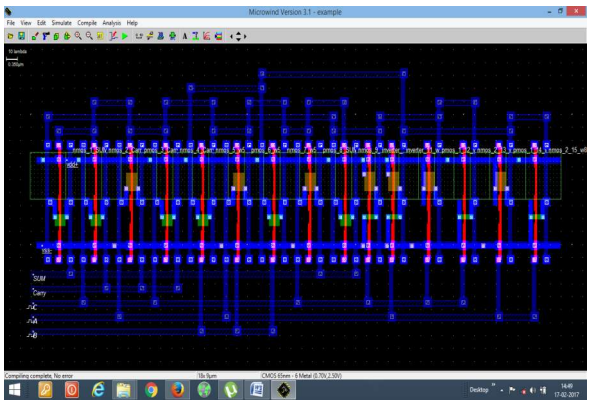

Figure 8 Layout of PTL & GDI Based Adder

5. IMPLEMENTATION OF ALU USING PTL AND GDI TECHNIQUE

After implementation of Full adder using ptl/gdi technique this adder can be used for implementing ALU, which also performs logical operation like AND, OR, XOR and Inverter. Implementation of Single bit ALU using PTL/GDI is shown in figure 9.But this implementation does not allow selection of operation, for this purpose we need 4:1 Mux which can be designed by using 2:1 Mux. And this Mux can then be used for Operation selection. Figure 10 shows Single Bit ALU with operation selection using 4:1 Mux implemented using PTL/GDI technology

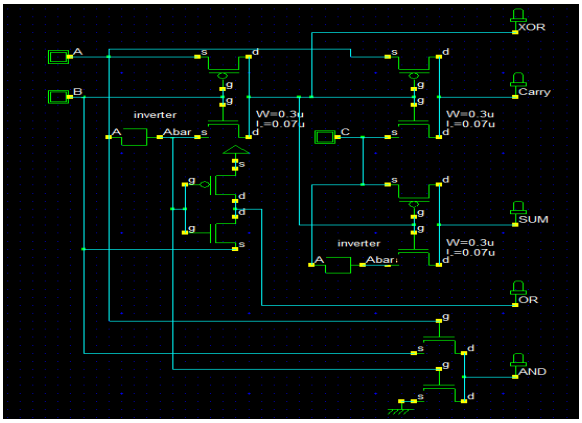

Figure 9 Single Bit ALU using PTL & GDI Technique

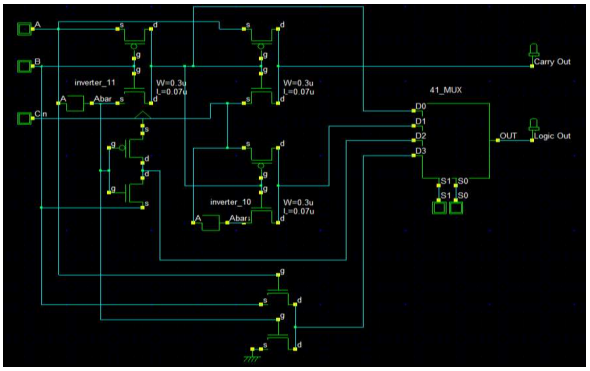

Figure 10 Single Bit ALU with MUX using PTL & GDI Technique

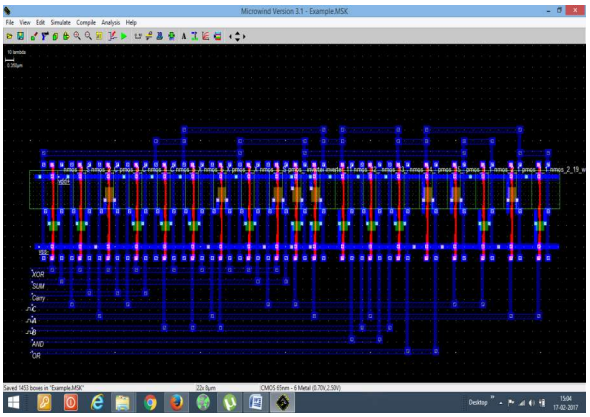

Figure 11 Layout of Single Bit ALU using PTL & GDI Technique

Table 1 Full Adder Analysis

COMPARITIVE ANALYSIS OF FULL ADDER

Parameter	Conventional Method (CMOS)	From Base Paper	Proposed Method
Number of transistors used	28.000	6.000	6.000
Delay time (ns)	0.610	0.360	0.320
Surface area	249.300	N/A	123.300
Power Dissipation (µ W)	25.146	3.600	16.306
PDP (nS.mW)	15.339	1.296	5.218

Table 2 ALU Analysis

COMPARITIVE ANALYSIS OF ONE BIT ALU

Parameter	Conventional Method (CMOS)	From Base Paper	Proposed Method
Number of transistors used	52	10	14
Delay time (ns)	92	50.8	4
Surface area	622.9	N/A	164.8
Power Dissipation (µ W)	124.07	4.47	19.7
PDP (nS.mW)	1141.4	227.076	78.8

6. CONCLUSION

This paper has presented the architecture design, logic design and circuit implementation of Single Bit ALU. The objective for Area, delay and power in ALU was carried out for bit operations using CMOS and PTL & GDI techniques and Comparison with CMOS Technique are shown in Table 1 & 2. The ALU designed with PTL & GDI technique gives less delay and less power dissipation with higher-speed of operation as compared to CMOS Technique.

7. ACKNOWLEDGMENT

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