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Novel Approach for Implementation and Optimization of Zigbee Transmitter

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Abstract**—***This paper shows the Verilog based design of digital transmitter for 2.4GHz band Zigbee applications. The paper proposes a design and implementation of 2.4GHz-band Zigbee transreceiver for an acknowledgement frame. The behavior of digital transreceiver is modeled using VHDL. The code is then synthesized, simulated and implemented on Spartan -2 FPGA. Improvement is attained in terms of performance and chip-area. The Zigbee transreceiver design meets theoretical expectations.*

Keywords:— *Zigbee, WPAN, VHDL, MAC*

1. INTRODUCTION

Zigbee is a specification for a suite of high level communication protocols using small, low-power digital radios based on an IEEE 802 standard for personal area networks. Zigbee devices are often used in mesh network form to transmit data over longer distances, passing data through intermediate devices to reach more distant ones. This allows Zigbee networks to be formed ad-hoc, with no centralized control or high-power transmitter/ receiver able to reach all of the devices. Any Zigbee device can be tasked with running the network. Zigbee operates in the industrial, scientific and medical (ISM) radio bands; 868 MHz in Europe, 915 MHz in the USA and Australia, and 2.4 GHz in most jurisdictions worldwide. Data transmission rates vary from 20 to 900Kbits/second. Zigbee builds upon the physical layer and medium access control defined in IEEE standard 802.15.4 (2003 version) for low-rate WPANs. The specification goes on to complete the standard by adding four main components: network layer, application layer, Zigbee device objects (ZDOs) and manufacturer-defined application objects which allow for customization and favor total integration. Zigbee is not intended to support power line networking but to interface with it at least for smart metering and smart appliance purposes. Because Zigbee nodes can go from sleep to active mode in 30 ms or less, the latency can be low and devices can be responsive, particularly compared to Bluetooth wake-up delays, which are typically around three seconds. Because Zigbee nodes can sleep most of the time, average power consumption can be low, resulting in long battery life.

ZigBee standard is developed by ZigBee Alliance, which has hundreds of member companies, from the semi-conductor industry and software developers to original equipment manufacturers and installers. The ZigBee alliance was formed in 2002 as a nonprofit organization open to everyone who wanted to join. The ZigBee standard has adopted IEEE 802.15.4 as its Physical Layer (PHY) and Medium Access Control (MAC) protocols. Therefore, a ZigBee compliant device is

compliant with the IEEE 802.15.4 standard as well.

ZigBee is a low-cost, low-power, wireless mesh networking standard. First, the low cost allows the technology to be widely deployed in wireless control and monitoring applications. Second, the low power-usage allows longer life with smaller batteries. Third, the mesh networking provides high reliability and more extensive range. ZigBee is a standard that defines a set of communication protocols for low data rate short range wireless networking. ZigBee based wireless devices operate in 868MHz, 915MHz and 2.4GHz frequency bands. ZigBee is targeted mainly for battery power applications where low data rate, low cost and long battery life are main requirements. In many ZigBee applications, the total time the wireless device is engaged in any type of activity is very limited. The device spends most of its time in power saving mode, also known as sleep mode. As a result, ZigBee enabled devices are capable of being operational for several years before their batteries needs to be replaced [3].

ZigBee standard is specifically developed to address the need for very low cost implementation of low data rate wireless networks with ultra low power consumption. The ZigBee Standard reduced the implementation cost by simplifying the communication protocols and reducing the data rate. The minimum requirements to meet ZigBee and IEEE 802.15.4 specifications are relatively relaxed compared to other standards such as IEEE 802.11, which reduces the complexity and cost of implementing ZigBee compliant transceivers.

2. OBJECTIVE

Zigbee Transmitter can be designed with analog components. Designing an analog transmitter is easier than digital. But in analog design, data transmission will be poor and the components also bigger and more. This will not allow accurate data transmission. In designing with digital, accurate data transmission will be obtained and power supply voltage range will be smaller. One way of designing digital Zigbee transmitter is with the help of Verilog HDL and VHDL through Xilinx. The objective is to design and to synthesis the Zigbee transmitter using Verilog which will result in lesser numbers of slices and Look-up-Tables (LUTs) utilized and lossless data transmission. With lesser number of components the power utilized shall be reduced.

3. EXISTING SYSTEM

The Zigbee digital transmitter is designed for an acknowledgment frame which is shown in Figure based on IEEE 802.15.4 standard. This is the simplest MAC frame format and does not carry any MAC payload. This frame is constructed from MAC header (MHR) and MAC footer (MFR). The frame control field and direct sequence number (DSN) form the MHR. The MFR is composed of 16-bit frame check sequence (FCS). Both MHR and MFR are known as PHY service data unit (PSDU), which becomes the PHY payload. The PHY payload is prefixed with the synchronization header (SHR) comprised of preamble sequence, start of frame delimiter (SFD), and PHY header (PHR). Together with the SHR, PHR and PHY payload form the PHY protocol data unit (PPDU).

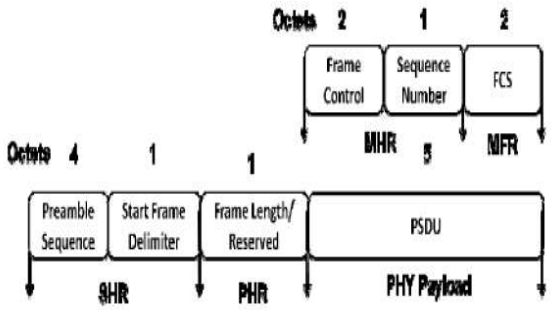

Figure 1:The Acknowledgement frame

4. LITERATURE REVIEW

[1] Sweatha Sankar T S, 2016, Zigbee standard consists of a set of communication protocols for wireless networking. This standard is suitable for communications with low power and low data-rate devices. This technology was dev loped for Wireless

Personal Area Networks (WPAN). Zigbee Alliance is the development authority of this standard. Zigbee standard is compliant with the IEEE standard 802.15.4 as well since it has adopted the Physical layer (PHY) and Medium Access Control (MAC) layer protocols of IEEE 802.15.4 standard.

[2] Anusha C.M, Kiran Kumar, 2015, This paper explores the implementation of a digital transceiver for 2.4 GHz Zigbee IEEE 802.15.4 applications for a given acknowledgement. Basically Zigbee was developed for a Wireless Personal Area Networks (WPAN), and aimed at control and military applications with low data rate and low power consumption..

[3] Punit Ramchandra Ramji, Manjunath G Asuti, 2014, This paper explores the implementation of a digital transmitter for 2.4 GHz Zigbee IEEE 802.15.4 applications on a field programmable gate array (FPGA) for an Acknowledgement frame

[4] A. Mohammed Mian and Divyabharathi, 2013, This paper explores Verilog design for various blocks in Zigbee Transmitter architecture for an acknowledgement frame. The word digital has made a dramatic impact on our society.

5. DESIGN METHODOLOGY

The behaviour of the Zigbee digital transmitter can be modelled using VHDL through Xilinx ISE. The VHDL module for each transmitter can be combined, then synthesized, simulated, and implemented on Spartan3E FPGA.

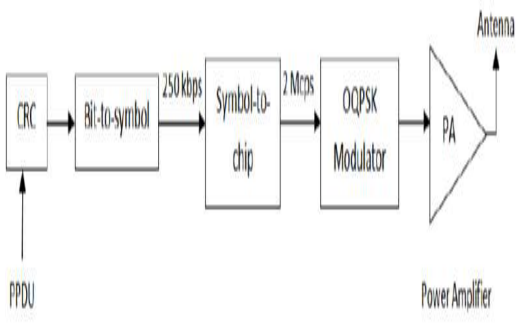

Figure 2: Transmitter Section

Cyclic redundancy check:

Error detection is the process of monitoring data transmission and determining when errors have occurred. Error-detection techniques neither correct errors nor identify which bits are in error – they indicate only when an error has occurred. The purpose of error detection is not to prevent errors from occurring but to prevent undetected errors from occurring. The most common error-detection techniques are redundancy checking, which includes vertical redundancy checking, checksum, longitudinal redundancy checking, and cyclic redundancy checking.

CRC Polynomial:

The most reliable redundancy checking technique for error detection is a convolutional coding scheme called cyclic redundancy checking (CRC). With CRC, approximately 99.999% of all transmission errors are detected. In CRC-16, 16 bits are used for the block check sequence. Here, the entire data stream is treated as a long continuous binary number. Because the Block Check Sequence (BCS) is separate from the message but transported within the same transmission, CRC is considered a systematic code. Cyclic block codes are often written as (n, k) cyclic codes where n = bit length of transmission and k = bit length of message. Therefore, the length of the Block Check Character (BCC) in bits is BCC = n – k (1) A CRC-16 BCC is the

Mathematically, CRC can be expressed as

$$\frac{G(x)}{P(x)} = Q(x) + R(x) \quad (2)$$

Where,

G(x) = message polynomial

P(x) = generator polynomial

Q(x) = quotient

R(x) = remainder

The generator polynomial for CRC-16 is

$$P(x) = x16 + x15 + x2 + x0 \quad (3)$$

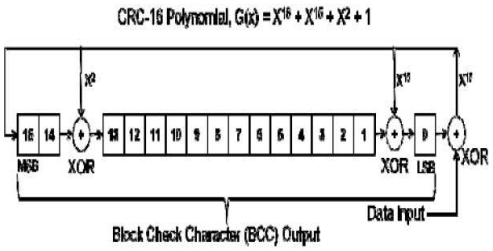

Figure 3: CRC Polynomial

6. SIMULATION AND RESULT

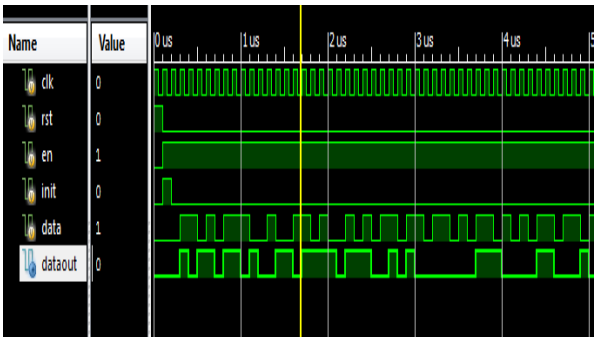

Figure 4 : Simulation for Transmitter

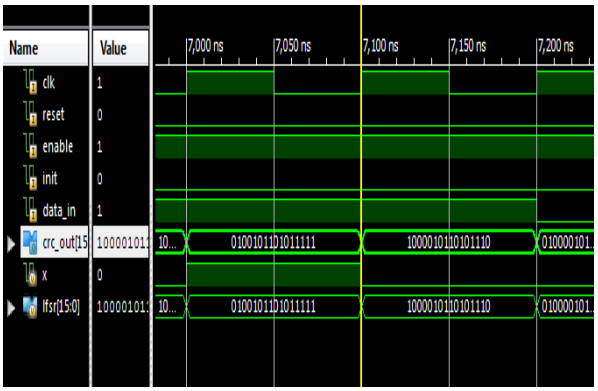

Figure 5: Simulation waveform for Cyclic Redundancy Checker

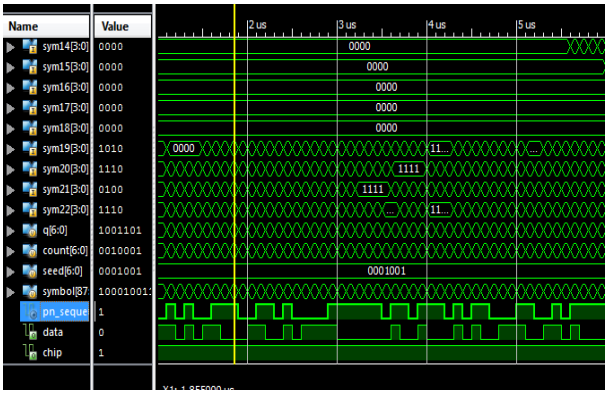

Figure 6: Simulation Waveform for Symbol to Chip

Synthesis Result:

Timing Summary:

Speed Grade: -4
Minimum period: 6.264ns (Maximum Frequency: 159.637MHz)
Minimum input arrival time before clock: 5.595ns
Maximum output required time after clock: 5.513ns
Maximum combinational path delay: 7.074ns

Area Report:

Selected Device: 3s100ecp132-4
Number of Slices: 182 out of 960 18%
Number of Slice Flip Flops: 280 out of 1920 14%
Number of 4 input LUTs: 173 out of 1920 9%
Number used as logic: 172
Number used as Shift registers: 1
Number of IOs: 6
Number of bonded IOBs: 6 out of 83 7%
Number of GCLKs: 1 out of 24 4%

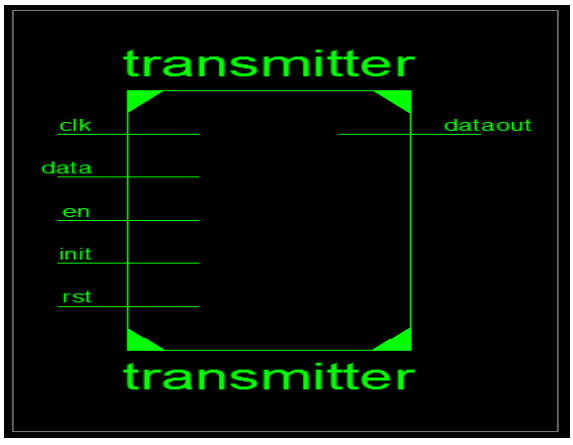

Figure 7 :RTL View of Transmitter

7. COMPARATIVE RESULTS

Table 1. Comparative results

S.NO.	Parameter	A. Mohammed Mian[4]	Result Obtained (Logic utilization)
1	Number of Slices	1%	18%
2	Number of 4 input LUTs	1%	9%

8. CONCLUSION

This paper shows the Verilog based design of digital transmitter for 2.4GHz band Zigbee applications. The behavior of CRC and Bit-to-symbol were characterized using Verilog as well as using VHDL. From the discussion, so far, part of the Zigbee transmitter is alone is characterized and synthesized. Both the results and synthesis report were compared and discussion has made for the design methodology. The remaining part of the transmitter will be designed and synthesized in future.

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