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Design & Implementation of Area and Speed Optimized FFT Processor Using New Vedic cum Wallace Multiplication Approach

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Abstract**—***Now days the digital circuitry has replaced most of the analog circuitry in various places because technically digital domain is much simpler than the analog domain. To operate these digital signals we use the Digital Signal Processors. In digital signal processing, to perform different types of operations we use various algorithms, out of these algorithms Fast Fourier Transform (FFT) is a significant algorithm for analyzing and performing digital computation of Periodic digital signals. Basically the FFT algorithm is used as an efficient means to compute the DFT and IDFT. This paper represents a new approach to design FFT algorithm for that we made some significant logics on the basic butterfly and reduce the total number of multiplication, as we knew the basically we need total four digital multiplication one addition and one subtraction for performing multiplication between two complex number's, our method has reduce that four digital multiplication into only three digital multiplication on cost of one extra addition and two extra subtraction, still it is a fair deal if we concern about area and speed. We also have proposal to have different categories of butterflies and FSM based FFT calculation to manage these categories.*

It is been proved that Vedic multiplication is the fastest multiplication approach but there are some other multiplication techniques which are even better than Vedic multiplication in terms of chip area. We have come up with the idea to merge two different multiplication techniques namely Vedic and Wallace and these gives us a fast and area efficient multiplication approach. Our proposed FFT algorithm is already efficient in respect of area and speed, all we need to optimize it further to have it we have plan to use our proposed Vedic cum Wallace multiplication technique on proposed FFT algorithm.

Keywords: *Finite State Machine (FSM), Discrete Fourier Transform (DFT), Inverse Discrete Fourier Transform (IDFT)*

1. INTRODUCTATION

Project Significance / Relevance with ongoing academic activities:-

As we are aware that any general purpose system (e.g. computer system) can perform lot's of computation and required software for different applications we just need to write some sort for software (program) for some sort of application and run that on General purpose system to get of expected outcomes, only problems with that system, is speed and the hardware, for small or big any application we have same hardware. Then the concept of ASIC and Embedded system comes into the picture that if we have specific application then why we go for general

purpose system, it's on us to choose, in embedded system we have different choices of microcontroller to select the best suitable for our application and in ASIC we can design our new hardware exclusive for the desired application, ASIC designing becomes simple because of FPGA's and HDL's so we can have our own design for our required application.

In field of DSP Transformation is prime requirement here we are proposing to design an IP (Intellectual Property) for the FFT. VLSI is all about Area, Power and speed, in our proposed design we have reduces the Area and get high frequency of FFT operations.

Transformation is a frequency analysis of time domain signals which further help us to design discrete/analog system (e.g. filters, modulators, demodulators etc.). FFT processor is widely used in different applications, such as WLAN, image process, spectrum measurements, radar and multimedia communication services. However, the FFT algorithm is a demanding task and it must be precisely designed to get an efficient implementation. If the FFT processor is made flexible and fast enough, a portable device equipped with wireless transmission system is feasible. Therefore, an efficient FFT processor is required for real-time operations and designing a fast FFT processor is a matter of great significance. In the past twenty years, FPGA has developed rapidly and gradually become universal. Compared with design flow of traditional ASIC, designs based on FPGA have the advantages of flexibility and high performance price ratio.

The VLSI design and Digital signal processing are one of the course subjects for B. E. and M. Tech. students, which deal with the designing of different digital circuits. By this project student will get better practical knowledge as well as their interest in the VLSI research will increase. This project will help students to experience real life DSP application.

2. PROJECT IMPACT - EXPECTED OUTCOME

FFT is a significant requirement when we deal with periodic digital signal and it is very useful in image processing, Radar, SAR (synthetic aperture radar) & multimedia applications. Our project will improvise the functioning of these systems. We are proposing to design and implement a new fast and area optimized FFT Processor, we are expecting faster multiplier then ref [1] and also we are expecting faster and more area optimized FFT processor as compare to ref [2] [3] [4].

3. LITERATURE SURVEY ON NATIONAL &INTERNATIONAL SCENARIO

In 2009 Dr. M. Ramalatha, *Senior Member, IEEE, has published a paper entitled"* High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques"[1] *in* IEEE *journal and proved that vedic multiplication technique is the fastest multiplication techniques till then. Later on in 2010 Dr.* Anvesh Kumar and Dr. Ashish Raman from NIT Jalandhar has published a paper entitled "Low Power ALU Design by Ancient Mathematics"[5] in IEEE explore and it was more power optimized then ref[1] with other parameters ware remains same. Later on in 2011 Dr. Harish M Kittur from VIT Vellore has published a paper entitled "Implementation of Vedic Multiplier for Digital Signal Processing"[6] in IJCA has used vedic multiplication techniques for DSP application and introduced CSA (carry save adder) combined with Vedic multiplication.

In 2010 Dr. Chen-Fong Hsiao & Dr. Yuan Chen, *Member, IEEE has published a paper entitled "*A Generalized Mixed-Radix Algorithm for Memory-Based FFT Processors"[2] in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS and proved that there module is best choice if area and speed concern till then. Later on in same year Dr. Ch. D. V. Paradesi Rao from JNTU, Hyderabad

published a paper entitled "An Area Efficient mixed-Radix 4-2 Butterfly with Bit Reversal for OFDM Applications"[3] in European Journal of Scientific Research for OFDM applications. Later on in 2012 Mr. G. Shafirulla and Mr. M. Subbareddy from VITS has published a paper entitled "Design of high speed FFT Processor Based on FPGA"[4] in IJMER and proved that there proposed FFT processor was batter then ref[2].

We have gone through all the references above and took them as base papers for our research work and proposed our design.

4. TECHNO-COMMERCIAL STATUS / OUTCOME / IPR / SOCIAL BENEFIT / OTHER

The measurement of running frequency is an important part of signals quality test. The standard signal method, analytic method and Fourier transform algorithm etc can be used for measurement of frequency. For the running power network, due to a variety of disturbances, anti-interfering and accuracy are necessary for the algorithm for frequency detecting. On one hand, the introduction of fast Fourier transform FFT algorithm brings the Fourier analysis from theory fields into applications, greatly improving the efficiency of Fourier transform, so that applications based on digital signal processing are developed rapidly. Under this condition, the Fourier transform algorithm becomes a reliable and effective algorithm for analysis of the grid frequency. However, the embedded processor resources are limited, and the design of algorithm depends on the capacity of processors. For FFT algorithm, most manufacturers only provide 64-point or less FFT assembly codes, and the following problem exists: for fixed sampling rate Fs and N-point FFT transform, the frequency resolution which can be reached is Fs/N. To enhance the resolution, the number of FFT processing points N shall be increased, causing larger calculation amount. Moreover, the existing efficient FFT assembly codes shall be modified, which increasing the difficulty of programming. On the condition of fixed sampling rate and N-point FFT algorithm, how to improve the frequency detection accuracy meeting the corresponding standard is the major subject of this thesis. Proposed FPGA based FFT algorithm sort out programming kind of problems in sort no programming needed. The FFT processor is one of the highest computational complexity modules in the physical layer of the IEEE 802.11n standard. According to IEEE 802.11n standard, the execution time of 64-point and 32-point with 1–4 simultaneous data sequences must be calculated within 3.6 or 4.0s. Therefore, if employing the traditional approach to solve the simultaneous multiple data sequences, several FFT processors are needed in the physical layer of a MIMO OFDM system. Thus, the hardware complexity of the physical layer in a MIMO OFDM system will be very high. This thesis proposes an FFT processor with a novel FSM based feedback architecture to deal with the issue of the multiple data sequences for MIMO OFDM applications. Furthermore, the power consumption can also be saved by using 2 point radix FFT algorithm.

Fast Fourier transform (FFT) are widely used in different areas of applications such as communications, radars, imaging, etc. One of the major concerns for researchers is the enhancement of processing speed. However according to use of portable systems working with limited power supplies, low-power techniques are of great interest in implementation of this block. FFT and IFFT blocks are used in OFDM links such as very high speed digital subscriber line (VDSL), Digital Audio Broadcasting (DAB) systems and microwave portable links. Of course there are many ways to measure the complexity and efficiency of an algorithm, and the final assessment depends on both the available technology and the intended application. Normally the number of arithmetic multiplications and additions are used as a measure of computational complexity.

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