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Design Low Power High Performance 8:1 MUX using Transmission Gate Logic (TGL)

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Abstract**—***In this paper, the primary and extremely engrossing issue within the low power VLSI circuits is Power dissipation. The fundamental approaches that we used for reducing power and energy dissipation in conventional CMOS circuits comprise reducing the power supply voltages, and minimizing the nodes, capacitances or switch activities with economical charge recovery logic. The various analyses are established additionally on Arithmetic circuits notably with multiplexer design. This paper also explores with Multiplexer to optimize the ability and designs an 8:1 Multiplexer with conventional CMOS Transistors and CMOS Transmission Gate Logic (TGL) which reduces the leakage power and leakage current in active mode. Transmission Gate Logic is used for reducing the circuit complexity as compared to the conventional CMOS based 8:1 Multiplexer. Transmission Gate Logic (TGL) based multiplexer circuit removes the degraded output and the PMOS and NMOS transistors are connected together for strong area output level. All the results of this paper are simulated on cadence virtuoso tool realized in 45nm technology with reduction of 4.688nW power, 2.762nA current and 0.7V supply voltage.*

Keywords:—*2:1 Multiplexer, 4:1 multiplexer, Transistor Gate Logic (TGL), Low Power, Leakage Circuit.*

1. INTRODUCTION

Multiplexer's square measure is a typical building block for data-paths, and is used extensively in a variety of applications together with the processors [1]. The low power consumption is one of the foremost vital problems within the system SOC design completely different techniques and technologies for low-power design in high-speed interface applications square measure developed and conjointly applied within the sensible designs [2]. There are numerous ways in which the square the measure is widely used for reducing the facility dissipation in circuits by reducing the change activities, offer voltage and load capacitances. These ways solely try and minimize the facility dissipation. However, still most of the energy down from DC power offer is totally dissipated within the circuit. The choice technique for reducing power dissipation is by the implementation of the adiabatic logic. The adiabatic logic circuits will scale back the facility dissipation up-to a massive extent by utilizing the AC power offer

for the utilization of the energy that holds on into the load capacitances instead of dissipating the energy with excessive heat within the circuit [3]. The electronic device circuit is usually accustomed to mix two or additional digital signals onto one line, by putting them there at completely different times. Technically, this can be referred to as time-division multiplexing. Multiplexers may be used as programmable logic devices [4]. The continual decrease in feature size of CMOS circuits and corresponding increase in chip density and in operation frequency have made power consumption a significant concern in VLSI design [5]. These communication systems want high-speed semiconductor devices at fiber or copper cable interfaces. Especially an electronic device (MUX) that is found in every transmitter should win an excellent operational speed as a result of its serial parallel information with an occasional bit rate into one information stream, with the utmost transmission rate within the system [6]. Multiplexer's square measure key has parts in CMOS memory parts and information manipulation structures. The increasing demand for considerably low-power massive scale (VLSI) has forced completely different design levels, like subject, circuit, layout, and therefore, the method technology level [7]. Functionally, Optical TDM (OTDM) is just like an electronic TDM. The sole distinction is that the multiplexing and operations square measure perform entirely optically at high speeds [8].

2. MULTIPLEXERS

Multiplexer is an important part in implementation of signal control systems and memory circuits [9]. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A Multiplexer in also called the data selector [10].

2:1 Multiplexer:

A 2:1 Multiplexer sends one of 2^n input lines to a single output line.

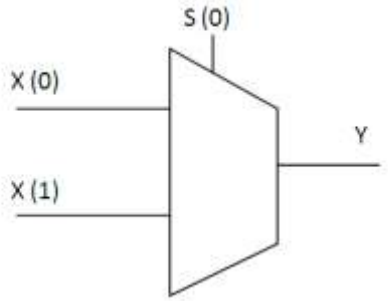
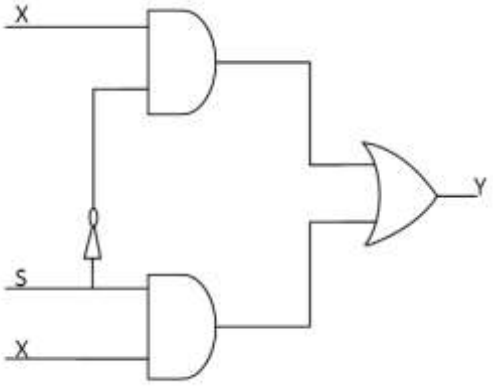


Figure (1): Conventional 2:1 MUX

A Multiplexer has two sets of inputs, X (0) & X (1) and one select line S (0). The Multiplexer output is in a single bit Y, which is one of the 2^n input data.

$$Y = S(0).X(1) + S(0).X(0) \quad \ldots. (1)$$



(a) Gate Implementation 2:1 MUX

S(0)	X(0)	X(1)	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(b) Truth Table of 2:1 MUX

Figure (2): (a) 2:1 MUX (b) Truth Table 2(b)

2 (b) 4:1 Multiplexer:

A Multiplexer sends one of 2^n input lines to a single output line.

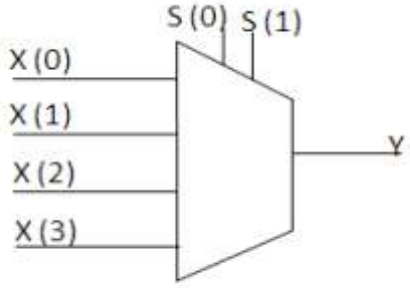


Figure (3): Conventional 4:1 MUX

A Multiplexer has four sets of input X (0), X (1), X (2), X (3) and two select lines S (0) and S (1). The Multiplexer output is in a single bit Y, which is one of the 2^n input data.

$$Y = X(0).\overline{S(0)}.\overline{S(1)} + X(1).\overline{S(0)}.S(1) + X(2).S(0).\overline{S(1)} + X(3).S(0).S(1) \quad \ldots (2)$$

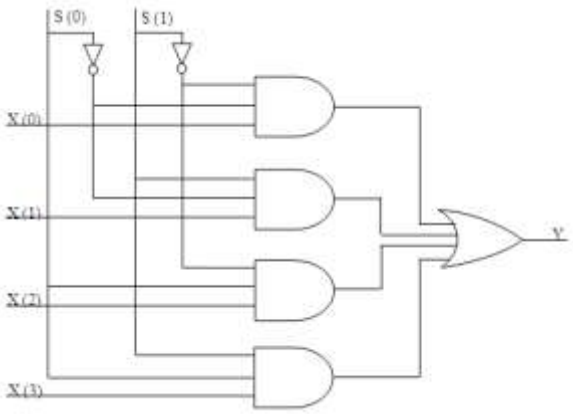


Figure (4): (a) Gate Implementation 4:1 MUX

S(1)	S(0)	Y
0	0	X(0)
0	1	X(1)
1	0	X(2)
1	1	X(3)

Figure (4): (b) Truth Table of 4:1 MUX

2(c). 8:1 Multiplexer: A 8:1 Multiplexer sends one of 2^n input lines to a single output line.

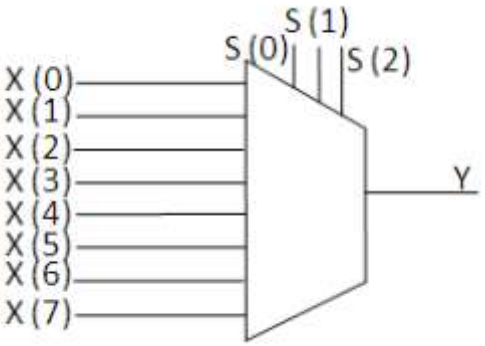


Figure (5): Conventional 8:1 MUX

A Multiplexer has eight sets of input X (0), X (1), X (2), X (3), X (4), X (5), X (6) and X (7) and three select lines S (0), S (1) and S (2). The Multiplexer output is in a single bit Y, which is one of the 2^n input data.

$$Y = X(0).\overline{S(0)}.\overline{S(1)}.\overline{S(2)} + X(1).S(0).\overline{S(1)}.\overline{S(2)} + X(2).\overline{S(0)}.S(1).\overline{S(2)} + X(3).S(0).S(1).\overline{S(2)} + X(4).\overline{S(0)}.\overline{S(1)}.S(2) + X(5).S(0).\overline{S(1)}.S(2) + X(6).\overline{S(2)}.S(1).S(0) + X(7).S(0).S(1).S(2) \quad \ldots (3)$$

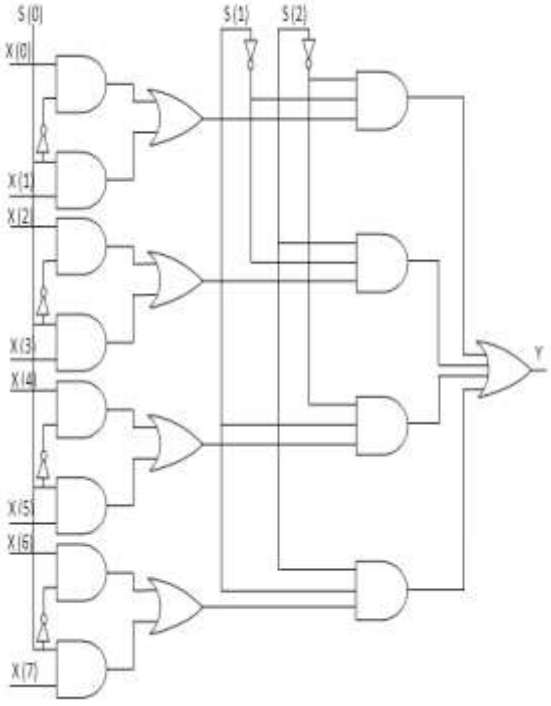


Figure (6): Gate Implementation 8:1 MUX

This circuit is conventional CMOS transistor level design of 8:1 MUX that consists of 126 transistors. It is the conventional circuit of the cadence tool using 45 nanometer technologies. Due to more transistors, the specified practicality will consume a lot of power with bumper space. But as the technology is reducing, the circuit ought to perform with minimum power consumption. As a result, this design is not thought of as advantageous for lower technology. The power consumption is reduced with minimum space in the proposed design [2]. The conventional CMOS transistor representation of an 8:1 MUX is shown in Figure. 7.

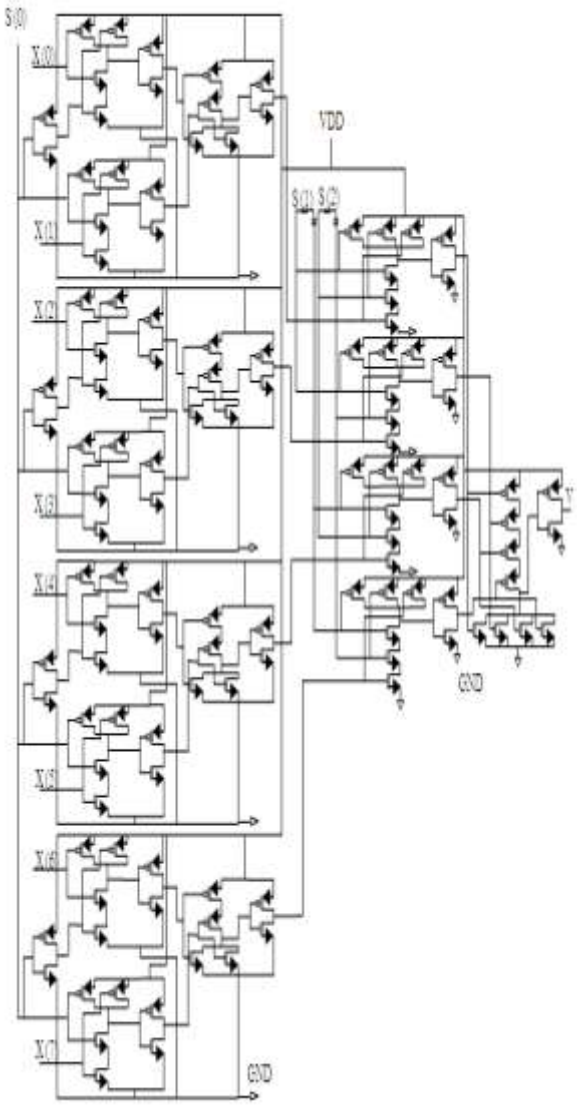
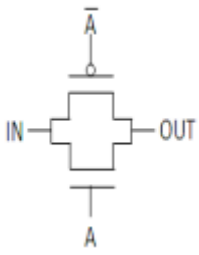


Figure (7): Conventional CMOS Transistor base 8:1 MUX

3. TRANSMISSION GATE LOGIC (TGL) BASED 8:1 MULTIPLEXER:



A	IN	OUT
H	H	H
H	L	L
L	X(don`t care)	Z(high imped-ance)

(a) *(b)*

Figure (8): (a) Transmission Gate (b) Truth Table

In this design, the transmission gate kind of MUX structure is enforced with terribly minimum transistors compared to the conventional CMOS primarily based design. The consecutive connected PMOS and NMOS arrangement acts as a switch and is thus referred to as transmission gate [11]. The transmission gates use 28 transistors as shown in Figure.9.

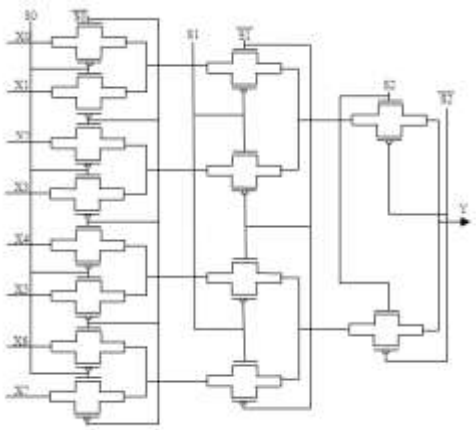


Figure (9): TGL base 8:1 MUX

NMOS devices pass a robust zero however a weak 1, whereas PMOS pass a robust one however, a weak 0. The transmission gate combines the simplest of each of the properties by inserting NMOS in parallel with the PMOS device [12-13]. Four transmission gates square measure are connected as in Figure. 9 to create an MUX structure. Each transmission gate acts as an AND switch to exchange the AND gate that is employed during a typical gate design of

MUX. Hence, the device count is reduced. The transmission gate primarily based 8:1 MUX is exhibited in Figure.9.

4. SIMULATION RESULT

In this section, the results of conventional and Transmission Gate Logic (TGL) type Multiplexer are calculated. Figure.10 shows the Transient Response of 8:1 Multiplexer.

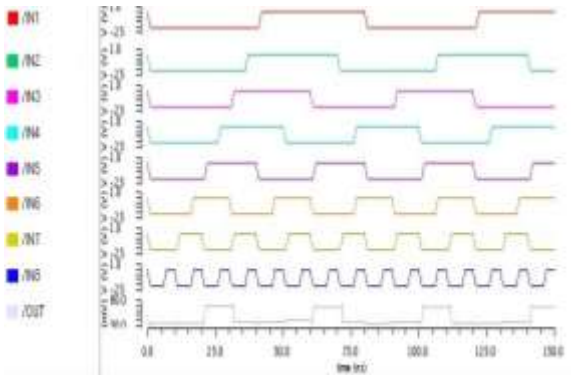


Figure (10): Input and Output of 8:1 MUX

Leakage Power: The leakage power or static, dynamic power dissipation is that in which the power dissipated within the circuit once is in standby mode only if the equation is as below [14-15].

$$Pleak = I\,leak \times VDD \quad \ldots 4$$

Where I leak is the leakage current that flows within the semiconductor unit once it is in OFF state and provides voltage VDD.

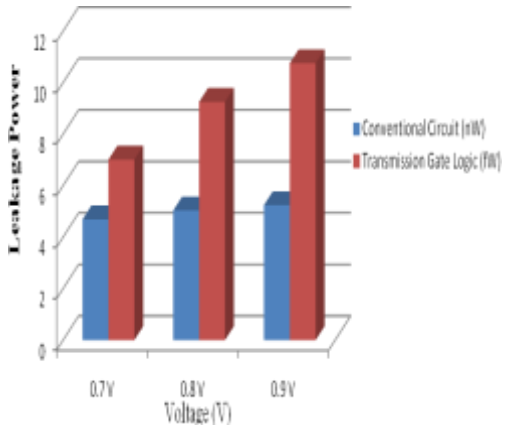


Figure (11): Leakage Power Comparison at Various Voltage Supplies

4.2. Leakage Current:

Leakage current consists varied parts of this [16]. Like the sub threshold leakage current, gate leakage current, reverse biased junction leakage current and gate evoked drain leakage current are The sub-threshold leakage current and also the gate leakage current square measure dominant within the circuit [17].

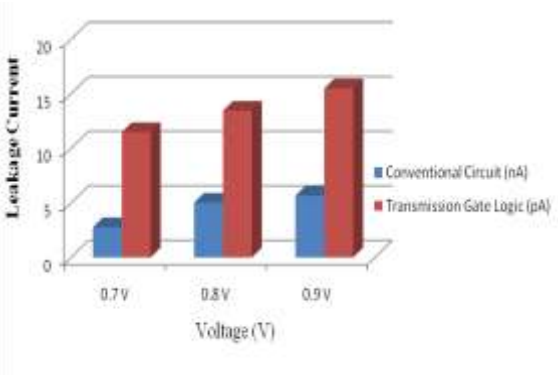


Figure (12): Leakage Current Comparison at Various Voltage Supplies

After the design of logic signal the delay is found to be imperative in every circuit. For this design, we need to find out the values of resistor that can introduce the delay on the signal lines. Delay of the circuit has depended on the value of the resistor itself as well as the capacitive load of the circuit [18]. The propagation delay of the RC circuit can be calculated by the Elmore model delay formula as follows:-

$$tp = 0.69Req \times CL \quad \ldots 5$$

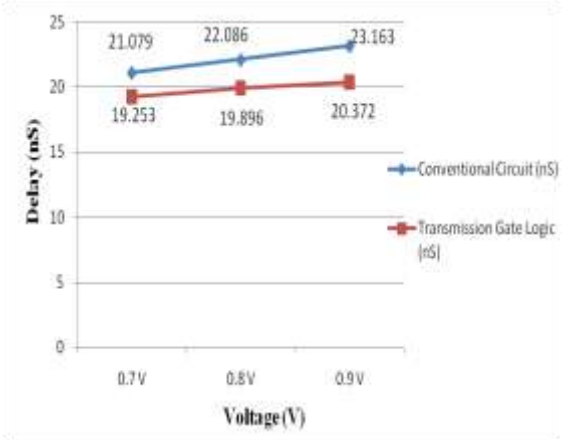


Figure (13): Delay Comparison at Various Voltage Supplies

5. COMPRESSION RESULTS

This section compares the result of Multiplexer Design.

Supply Voltage	Conventional Circuit			Transmission Gate Logic (TGL)		
	Delay (nS)	Leakage Current (nA)	Leakage Power (nW)	Delay (nS)	Leakage Current (pA)	Leakage Power (fW)
0.7	21.079	2.762	4.688	19.253	11.48	7.01
0.8	22.086	5.021	5.031	19.896	13.45	9.25
0.9	23.163	5.657	5.236	20.372	15.50	10.75

6. CONCLUSION

This paper has proposed designs for reduction of leakage power and leakage current the 8:1 Multiplexer design with two types of conventional CMOS Transistors and Transmission Gate Logic (TGL), the conventional circuit design with 126 transistors and Transmission Gate Logic (TGL) with 28 transistors. Power consumption and current of TGL circuit is much less as compared to the conventional circuit and the number of transistors is also much less as compared to the conventional circuit. The result is calculated in active mode with voltage variation. The 8:1 Multiplexers were designed using 45nm technology on cadence virtuoso tool. Using this tool the results are calculated. Leakage power of conventional 8:1 MUX is 4.688nw and Transmission Gate Logic (TGL) is 7.01fw. The leakage current of conventional circuit is 2.762nA and TGL circuit is 11.48pA only.

7. ACKNOWLEDGEMENT

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