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Enhancement of Parameters for Non-Volatile SRAM Cell using Memristor

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Abstract—In today's electronics world, power is a most important problem in the system on chip (SOC) design at the nanometer level. The maximum portion of chip region is embedded by the memory part that's why it is obligatory to control dissipation of power in cache or temporary storage memories. In the past to control the power dissipation, researchers have introduced the low power circuits for volatile memories but data retention is a critical problem in volatile memories like SRAM which increases the booting time for a circuit operating SRAM as their main or cache memory. This gives rise to the birth of the non-volatile memories like memristor based SRAM's (NVSRAM) to restore data after power off. This deals with the data retention which automatically reduces the usage of power. In this paper, low power non-volatile memristor based SRAM cell i.e., 4T2R SRAM cell is proposed and also a comparison of parameters of proposed NVSRAM with a conventional 6T SRAM is discussed. After the simulation of the proposed SRAM cell, significantly declination in power dissipation is observed. Simulation results show that various parameters like leakage current, leakage voltage, leakage power, power and a delay of proposed Non-volatile SRAM (NVSRAM) cell are better than the SRAM cell.

Keywords:— *SRAM, low power, memristor, delay.*

1. INTRODUCTION

In digital electronic devices the memories are very important. We know that it occupies the maximum area of the chip. Therefore to reduce the area of the chip, we need to manage the function of that chip to be same. For this, there is a need to add the required number of transistors to balance the function of that chip, which automatically requires excess power to run the system. Therefore, this consumption of power has happened to be a complexity for designers. So, it's very necessary to control the utilization of power from the memory part for enhancing the system's functioning [4]. Then designers designed low power volatile memories like Static random access memory (SRAM). Here, we consider the 6T SRAM cell. The problem with the SRAM is the data retention i.e., they are unable to bring back the data after power off operation which increases the booting time of the system, obviously, that consume some more power. Then after so many researches, designers introduced Non-volatile memory which retains the data after the power cut down. Nowadays, the most trending non-volatile memory is the Memristor-based SRAM which is also known as Resistor random access memory (RRAM). The RRAM is more stable compared to the SRAM because of its non-volatile nature. A Memristor (memory + resistor) is a fourth elementary circuit component, which can change its

internal resistance according to the voltage applied across the terminals. It can be used as the memory because of its non-volatile characteristics [1]. Memristor is a fourth fundamental missing circuit component introduced by Leon Chua in 1971 [2]. The resistor, capacitor and inductor are the remaining basic circuit elements. In 2008, Hewlett Packard lab affirmed that Memristor is manufactured physically utilizing two terminal titanium-di-oxides (TiO_2) [3]. HP lab cleared up the primary physical showing of a memristor, fitting in with Chua's hypothesis [6] and trending in the electronics industries. A Memristor is a two-port component works in one of the two resistive states RON and ROFF according to the operation of the cell, which are non-volatile in nature. So, it consumes a minimum amount of power than transistors as they don't require a minimum voltage to detect their state as well as there's no need of power to retain the data [5]. There is a good advantage with the memristors because of its great compatibility with the CMOS circuits.

The rest of the paper is organized as follows. Section II introduces the behaviour and working of the volatile 6T SRAM cell. Section III explains the origin and operation of the memristor. Section IV includes the proposed non-volatile SRAM cell using Memristors. Section V discusses the results and section VI represents the conclusion part.

2. MEMRISTOR

The memristor theory was developed in 1971 by Professor Leon Chua [1]. The memristor is similar to a resistor however it can change its internal resistance depending upon the voltage applied across the two terminals. At the point, when there is no applied voltage or the power supply is turned off then it memorizes its past state which makes it perfect for non-volatile memory purpose [7]. During circuit operation, the memristor is used to be in either R_{ON} or R_{OFF} resistive states. The relation between magnetic flux and the charge gives rise to the operation of the memristor. The symmetric relation between resistance, capacitance, inductance and memristance is described in Figure .

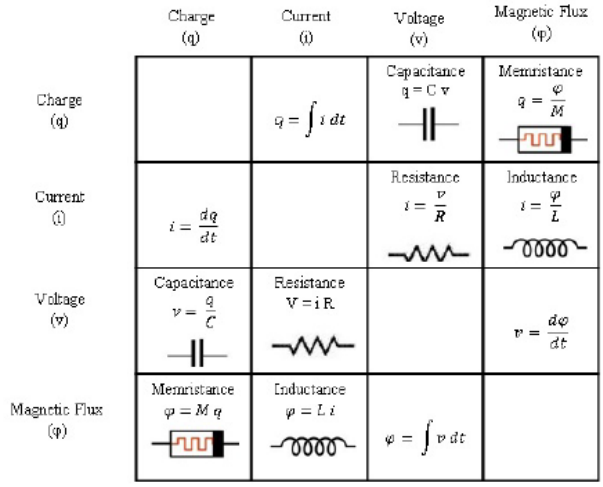

Figure 1. The symmetric relation between the resistor, capacitor, inductor and Memristor.

The circuit of the memristor is shown in Figure 1. Memristor is a nano-sized device. It consists of a thin film of 5nm thickness with one layer of insulating TiO_2 and one layer of reduced oxygen TiO_{2-x}, which are surrounded by platinum wires. The Tio_{2-x} ions behave like dopants due to the oxygen vacancies which produces the doped region. The resistance of this doped region is considerably lower than the un-doped region [9]. Simply, we can say memristor is the combination of the low doped area and a high doped area with the high resistance (R_{OFF}) and low resistance (R_{ON}) respectively shown in Figure . Therefore, it can be viewed as two resistors with different resistivity connected in series, which is shown in Figure 1. It is explained by the equation 1.

$$RM\,(x) = x(t)RON + [1 - x(t)]ROFF \qquad (1)$$

Here, w(t) indicates the width and (D) indicates the substantial length of the memristor. This is given by

$$x(t) = {}^{w(t)}/_{D} \qquad (2)$$

The consumption of power by memristor is very less as they don't require a power supply to restore the data. That's why it is more preferable than the transistor [8]. To deal

with the memristor, we should calculate the memristance. This is expressed as

$$M = \frac{d\phi}{dq} = \frac{vdt}{idt} = \frac{v}{i} \qquad (3)$$

Above expression is related to the Ohm's law. Therefore, simply memristance can be defined as a linear relationship between the current and the voltage as long as M does not change along with the charge [4]. The consumption of power by a memristor is given by

$$p(t) = I^2R = I(t)V(t) = I^2(t)M(q(t)) \qquad (4)$$

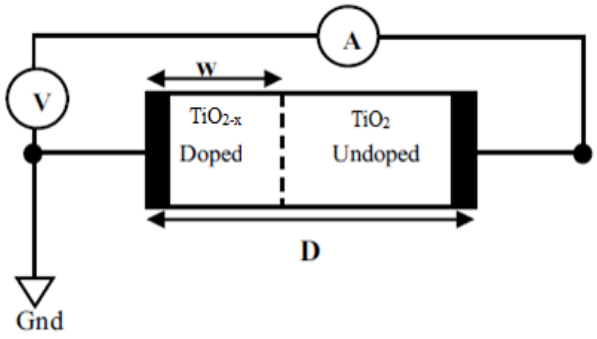

Figure 2. Memristor Structure.

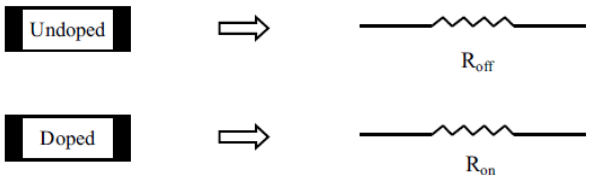

Figure 3. Regions with resistances.

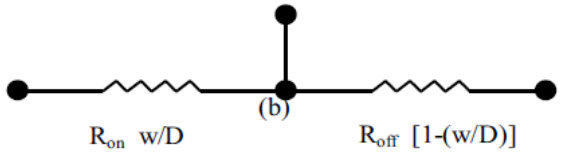

Figure 4. Resistances in series.

3. CONVENTIONAL 6T SRAM CELL

The 6T SRAM cell is acknowledged as the CMOS standard SRAM cell because of its characteristics of high switching, good SNM and low power dissipation [10]. As exposed in Figure 5., the 6T SRAM cell is the combination of two cross-coupled inverters with the two access transistors allied to a complementary bit lines i.e., BL and $\overline{BL}$ with a power supply V_{DD} of 0.7V. The data present in the cell is controlled by access transistors. This cross-coupled inverter acts like a bi-stable latching circuitry to store '0' or '1' [11]. The SRAM design should be made in such a way that the data which is read from or write through bit lines should not be disturbed [12]. During a write operation, the data is given at BL and BLB which acts like input signals. If BL = '0', then $\overline{BL}$ = '1' or vice-versa. The word line is set to high and then the access transistors get activated. Therefore, data from bit lines will be written into the cell [13]. For a perfect write operation, the pull-up ratio i.e., the ratio of) $\frac{W}{L}$ of load transistor to the ($\frac{W}{L}$) of the access transistor should be small [14]. As the word line is high, data in the cell is going to be read with the help of bit lines. During this operation, the voltage values present at the bit lines will be sent to the sense amplifier which acts as a comparator and then finally gives the output [15]. Read stability is important in the design of SRAM cell [16]. Simply, whenever the word line WL gets low then the cell used to be on standby or hold mode. The size of the access transistors should be set in a way such that it should be smaller than pull-down transistors and greater than the pull-up transistors to attain stability and a higher performance [17].

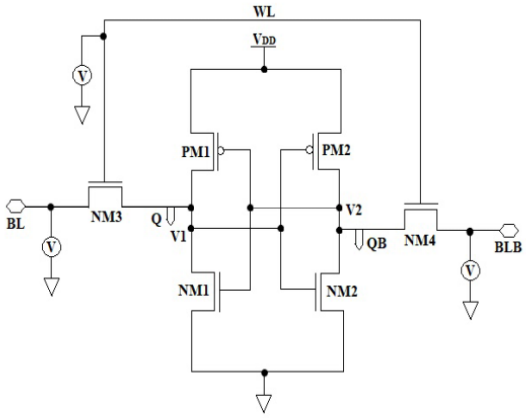

Figure 5. Schematic of a Conventional 6T SRAM cell.

4. PROPOSED NON-VOLATILE 4T2M SRAM CELL

As we know that due to volatile memories, we are facing a major problem i.e., power dissipation caused due to the more booting time to hold the data constantly. To overcome this, researchers are dealing with the non-volatile memory. This results in the production of different non-volatile memories. An addition of memristor to volatile memories like SRAM forms it into a non-volatile SRAM. So in this paper, we designed a Non-volatile 4T2M SRAM cell. The proposed non-volatile SRAM cell (NVSRAM) is represented in Figure 6 (a). It is obtained by replacing two PMOS transistors in a 6T SRAM cell with two memristors (M_1 and M_2). As you observe in the figure, both memristors M_1 and M_2 are parallel to each other and they connected to transistors NM_1 and NM_2 respectively.

Let's see the function of the proposed non-volatile SRAM cell. Initially, power is ON and the current flows in the forward direction making both memristors to a high bias state. When the cell is discharging, the current runs in reverse direction through one of the memristors making it to a low bias state. The memristor used to be in low bias state during the power-off time. Due to this different flow of currents, the resistivity mismatch takes place. This mismatch leads to storage of data. That's why we called it as non-volatile. When the power is on, then the mismatch brings back the stored data or restores the data by the latch mechanism. In this situation, the memristor having the low bias state contains the high voltage compared to the other memristor [18]. During the write operation, the data is given at output nodes Q and $\bar{Q}$ through the bit-lines BL and $\overline{BL}$ respectively. According to the stored data, the memristance of memristors changed to either High resistance state (HRS) or low resistance state (LRS). Let's consider during a write operation, the data stored at Q and $\bar{Q}$ be '1' and '0'as shown in Figure 6 (b). Due to this, transistor NM_2 gets enabled and then current flows through the positive polarity of M_2 and negative polarity of M_1. As you observe in the figure, there is a forward current through M_2 and reverse current through M_1. Then the memristance of M_1 is converted to LRS and M_2 is converted to HRS as shown in Figure 6 (c). In the same way, if the data stored at nodes reversed, then the state of memristors will also get inverted. During a read operation, the data stored at outputs Q and $\bar{Q}$ gets read by taking the differentiation of voltages at BL and $\overline{BL}$ respectively and sending it to the sense amplifier [19].

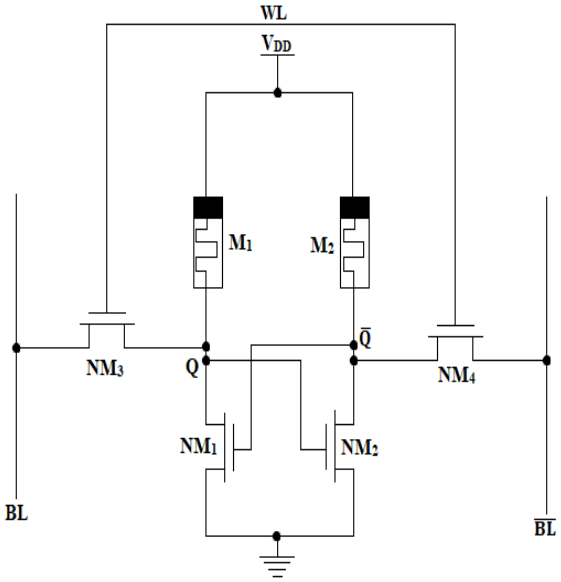

Figure 6 (a). Non-volatile SRAM cell with memristors.

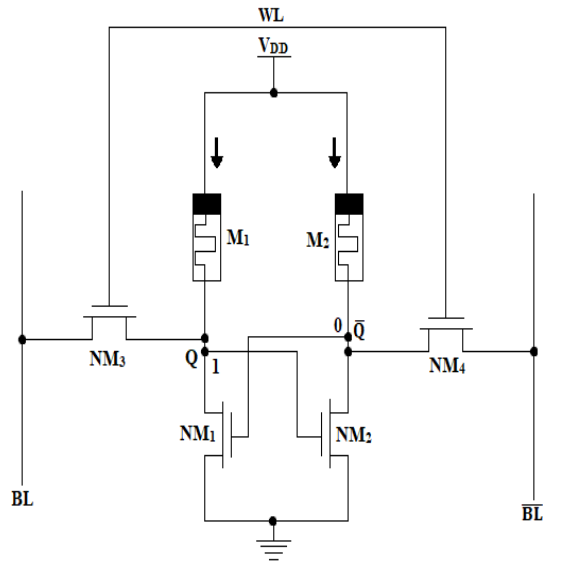

Figure 6 (b). Data is stored

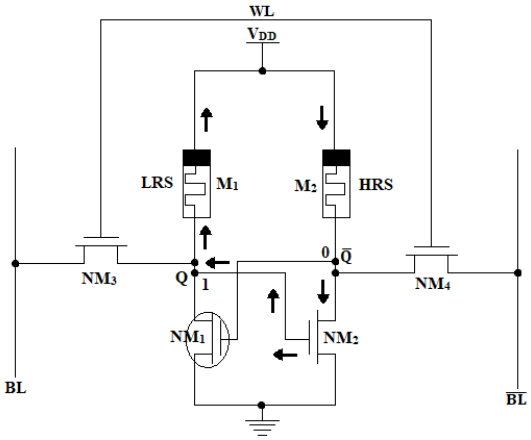

Figure 6 (c). Memristors with their different resistivity levels due to forward and reverse currents.

5. RESULTS AND SIMULATIONS

A. 6T SRAM cell output

The transient response of conventional 6T SRAM is done in 90nm Cadence technology is shown in Figure 7. If you observe in the figure, the data given at bit-lines (BL and) $\overline{BL}$ are 0 and 1 respectively by making the word-line high. Here, the data has been written into the cell at Q and $\bar{Q}$ through access transistors. The written data can be read by pre-charging both the bit-lines (BL and) $\overline{BL}$ to V_{DD} maintaining word-line high.

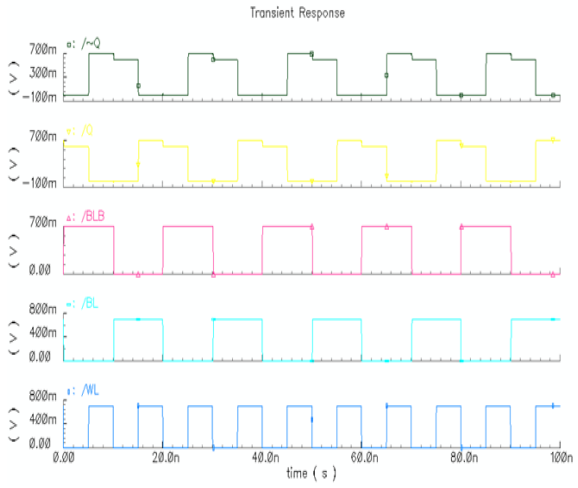

Figure 7. Transient response of 6T SRAM cell.

B. 4T2M SRAM Output

A Verilog-A model for the memristor has been developed and added to the library of cadence to undergo simulations with CMOS circuits. In this model, we have given the fixed values of the parameters of the memristor. They are R_{ON} = 100Ω, R_{OFF} = 20KΩ, D = 3nm and μv = 350×10^{-9} $m^2/s/V$ where R_{OFF} and R_{ON} represents the high resistance state and low resistance state respectively. D defines the thickness of film and μ defines the portability of dopants in the thin film [20]. The flow of forward and reverse currents through memristors leads to the formation of R_{ON} and R_{OFF} states.

The transient response of memristor-based NVSRAM is shown in Figure 8. Here, the data is written into the cell following the same process as applied for 6T SRAM cell. As you observe in 6T SRAM output, the data written into the cell has been read but when the power is OFF, then data becomes lost. In the sense of memristor-based SRAM cell, we will consider power off condition as WL low condition in order to understand the graph. When we observed in this cell output, the data present in the cell won't get lost when the WL goes low. The data has been maintained constantly and was restored when the power is ON. By this, the stability of this cell will be far better than the 6T SRAM cell. There will be less leakage current, less leakage voltage, less power consumption and the less delay time relative to the conventional 6T SRAM cell.

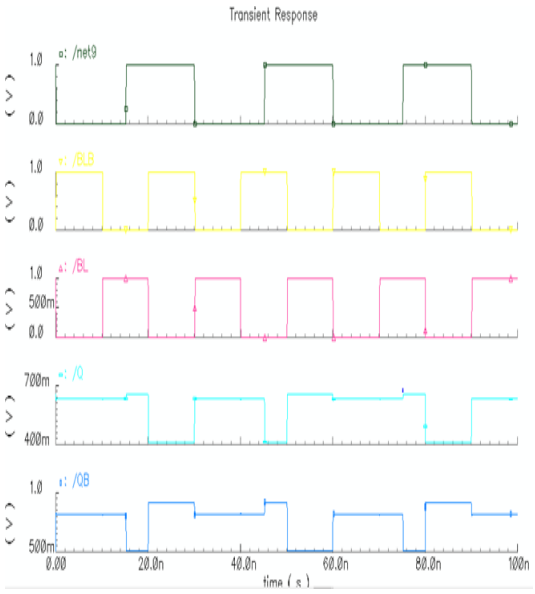

Figure 8. Non-volatile 4T2M SRAM cell.

Power

The total power consumed by the cells during the processing of data is calculated. According to the results, the power consumption is more in 6T SRAM than compared to the NVSRAM.

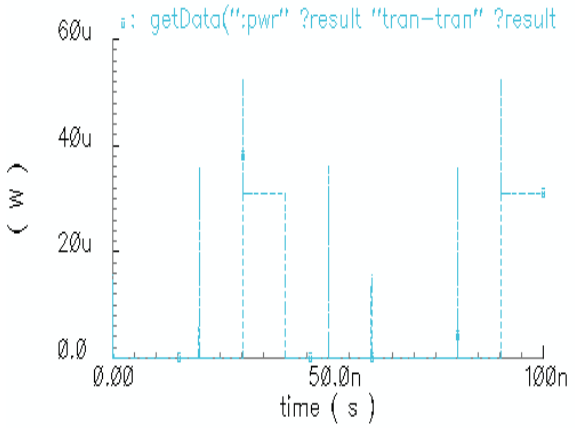

Figure 9. Power graph of Conventional 6T SRAM cell.

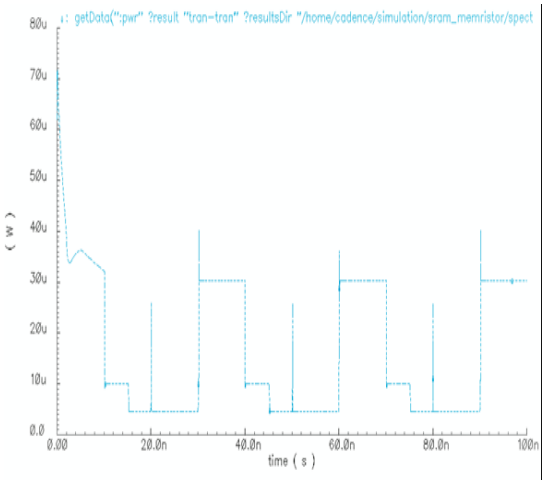

Figure 10. Power graph of proposed NVSRAM cell.

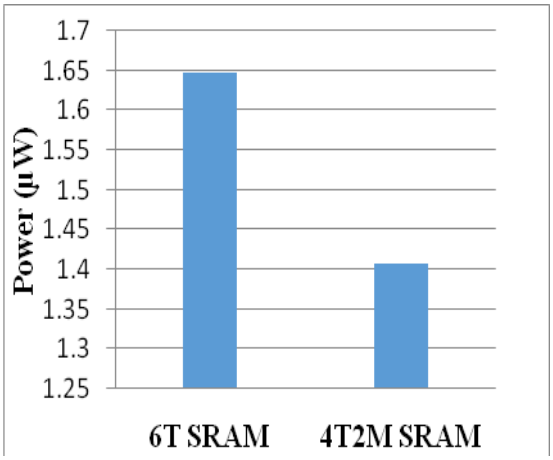

Figure 11. Comparison of power consumption of both cells with the power supply of 1V.

Leakage Current

Due to scaling in technology, the leakage current increases continuously. It is the unwanted current in the cell and main responsible for the power dissipation. As we know that, the power dissipation is more in volatile SRAM cell than the proposed non-volatile SRAM cell, therefore there will be less leakage current in proposed NVSRAM cell relative to the 6T SRAM cell. By observing the below table results, it was proved that the proposed cell has less leakage current relative to the 6T SRAM cell.

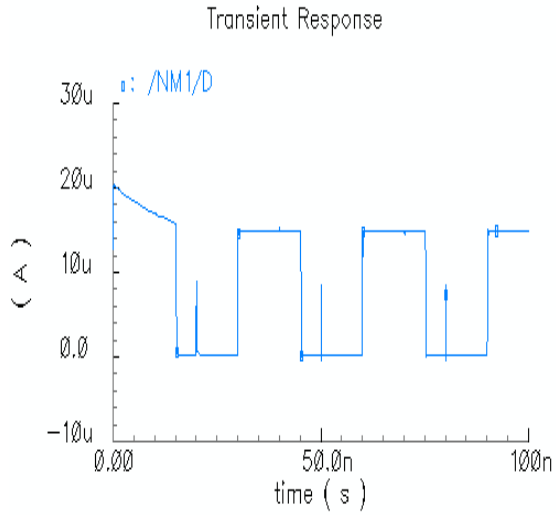

Figure 12. Leakage current for 6T SRAM cell.

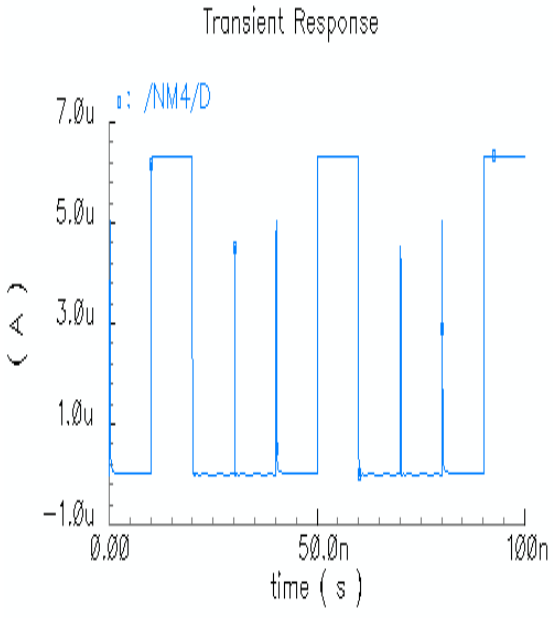

Figure 13. Leakage current for 4T2M SRAM cell.

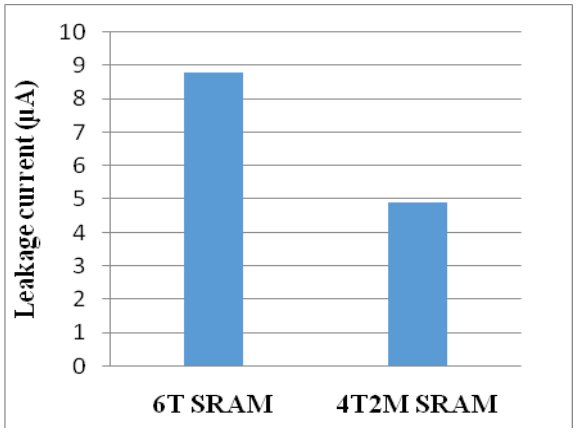

Figure 14. Comparison in Leakage current of both cells with power supply voltage 1V.

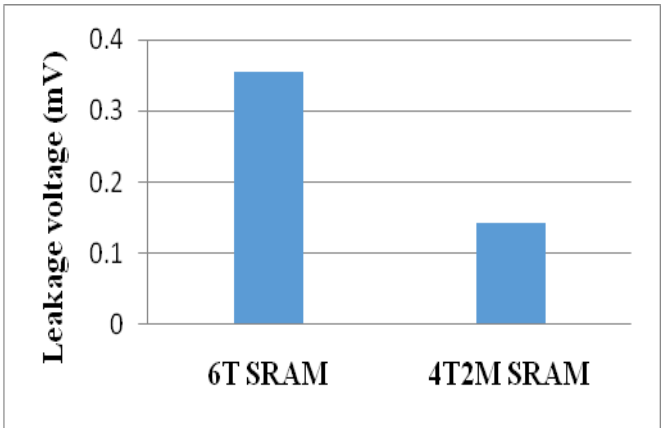

Figure 17. Comparison of leakage voltage of both cells.

Leakage voltage

Leakage voltage is the voltage which is wasted when the circuit is processing the data. Due to this, there will be a great loss of power. So, it is very important to take care of the voltage. As you observed from the simulation results, the leakage voltage of the 4T2M SRAM cell is less than the normal volatile SRAM cell. This is all due to its non-volatile nature.

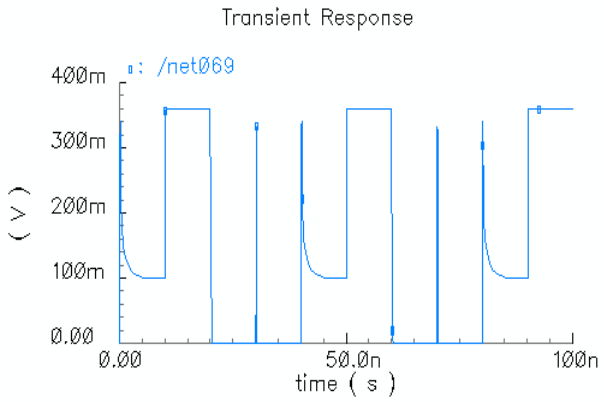

Figure 15. Leakage voltage for 6T SRAM cell.

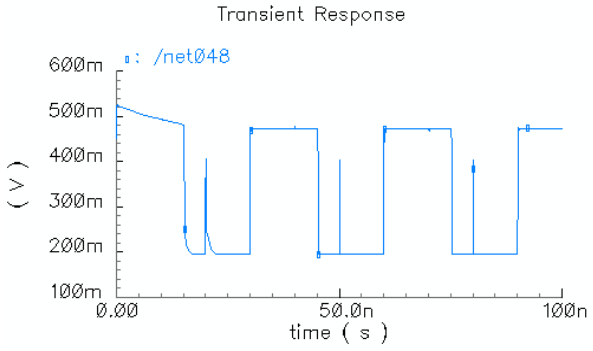

Figure 16. Leakage voltage for 4T2M SRAM cell.

Leakage power

Leakage power is due to the leakage current that does not contribute to the cell function. The unwanted threshold current in the cell when the transistor is turned off gives birth to this leakage power. In this paper, it is clearly proved that leakage power is more for 6T SRAM than compared to proposed NVSRAM cell.

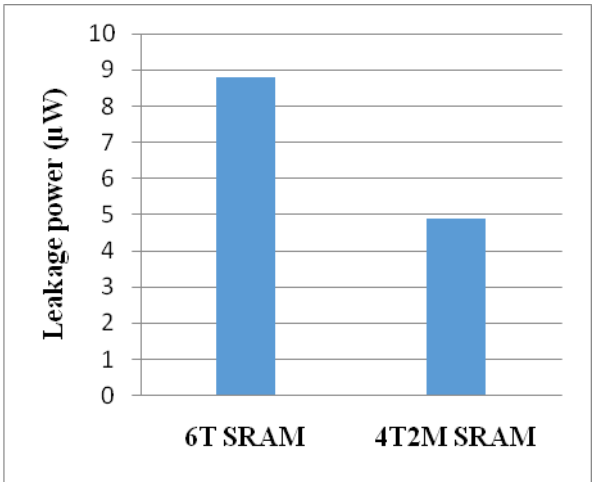

Figure 18. Comparison of leakage power of both cells.

Delay

The average of rise time and fall time between the input and output is known as a delay. By delay, we can judge the speed of processing of that circuit. In this case, if delay increases, then the processing speed of the SRAM cell decreases and vice-versa [21]. As proposed SRAM cell contains non-volatile nature, its delay is small relative to the conventional 6T SRAM cell.

Table 1. Comparison of the Time Delay for Different SRAM Cells.

Different SRAM cells	Delay (ns)			
	Input	Output	Input	Output
	BL	Q	BLB	QB
6T SRAM	40.04		81.25	
4T2M SRAM	33.02		52.17	

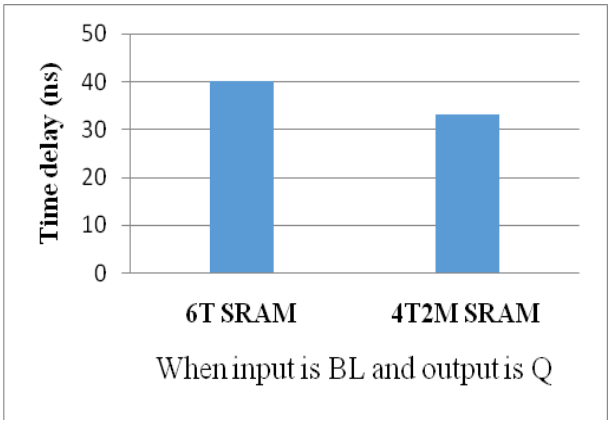

Figure 19. Comparison in time delay for both cells, when BL acts as input and Q acts as an output.

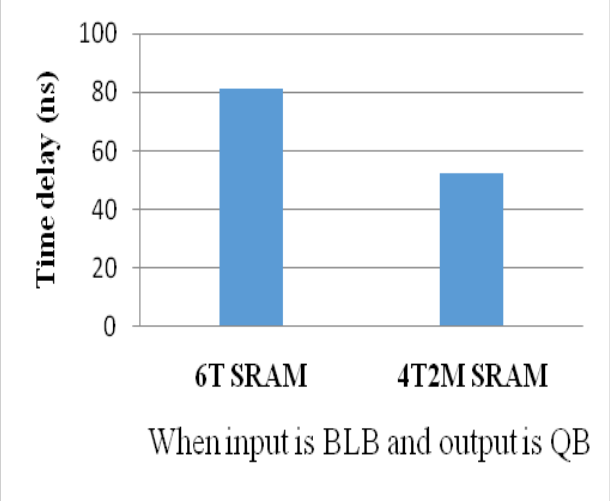

Figure 20. Comparison in time delay for both cells, when $\overline{BL}$ *acts as input and* $\overline{Q}$ *acts as output.*

Table 2. Comparison of Overall Results.

Different cells	Power (µw)	Leakage current (µA)	Leakage voltage (mV)	Leakage power (µW)
6T SRAM	1.6484	8.8104	0.3547	8.8104
4T2M SRAM	1.4071	4.8959	0.1422	4.8959

CONCLUSION

In this paper, we have designed a low power based Non-volatile 4T2M SRAM cell with the help of memristors using cadence gpdk90nm CMOS technology. We have compared the working of proposed non-volatile SRAM cell with the volatile 6T SRAM cell and power dissipation in both of them. We did a comparison between them on the basis of parameters such as leakage current, leakage voltage, leakage power, power and delay. By the above results, it is clear that values of all parameters for the proposed NVSRAM cell are lesser than the conventional 6T SRAM cell. This is all because of the data retention present in the 4T2M SRAM cell which leads to less booting time than compared to conventional SRAM cell. So, we can say that the power dissipation is more in 6T SRAM cell than compared to the proposed NVSRAM cell. Therefore, the non-volatile SRAM cell has more stability than the 6T SRAM cell. By this we can say non-volatile memories are more preferable than the volatile memories. Because of this, in coming generations the transistors in CMOS technology are going to be replaced by the memristors which are nanosized occupies the sufficient area on the chip and saves the power.

6. ACKNOWLEDGEMENT

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REFERENCES:

[1] B. Mohammad, D. Homouz, and H. Elgabra, "Robust Hybrid Memristor-CMOS Memory: Modeling and Design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 11, pp. 2069–2079, 2013.

[2] L. Chua, "Memristor-The missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971.

[3] Strukov, Dmitri B., et al. "The missing memristor found." nature 453.7191 (2008): 80.

[4] A. Jadon and S. Akashe, "Hybrid CMOS-memristor 4T-NVSRAM cell for low power applications," *2014 Innovative Applications of Computational Intelligence on Power, Energy and Controls with their impact on Humanity (CIPECH)*, 2014.

[5] V. Saminathan and K. Paramasivam, "Design and Analysis of Low Power Hybrid Memristor-CMOS Based Distinct Binary Logic Nonvolatile SRAM Cell," *Circuits and Systems*, vol. 07, no. 03, pp. 119–127, 2016.

[6] Chen, G. (2008) Leon Chua's Memristor. IEEE Circuits and Systems Magazine, 8, 55-56.

[7] Mem. Panwar, Mahendra Singh, and Mr Amit Kumar. "Design and Implementation of Non-Volatile SRAM using Memristor." Imperial Journal of Interdisciplinary Research 3, no. 7 (2017).

[8] L. Chua, "Resistance Switching Memories are Memristors," *Memristor Networks*, pp. 21–51, 2014.

[9] N. Gupta, H. Pahuja, B. Singh, and N. Nagpal, "A novel design of low power nonvolatile 10T1R SRAM cell," 2016 5th International Conference on Wireless Networks and Embedded Systems (WECON), 2016.

[10] G. Prasad and R. Kusuma, "Statistical (M-C) and static noise margin analysis of the SRAM cells," 2013 Students Conference on Engineering and Systems (SCES), 2013.

[11] T. S. Geethumol, and K. S. Sreekala "Read Stability Analysis of 6t SRAM Bit Cell", International Journal of Recent Trends in Engineering & Research (IJRTER), vol. 02, no. 05; pp. 2455-1457, 2016.

[12] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies," *IEEE Journal of Solid -State Circuits*, vol. 41, no. 11, pp. 2577–2588, 2006.

[13] P. Mishra, E. John, and W.-M. Lin, "Static noise margin and power dissipation analysis of various SRAM topologies," *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2013.

[14] K. Khare, R. Kar, D. Mandal, and S. Ghoshal, "Analysis of leakage current and leakage power reduction during write operation in CMOS SRAM cell," *2014 International Conference on Communication and Signal Processing*, 2014.

[15] I. Rizvi, Nidhi, R. Mishra, and M. S. Hashmi, "Design and analysis of a noise induced 6T SRAM cell," *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, 2016.

[16] S. Akashe, V. Rajak, G. Sharma, and S. Sharma, "Enhancement of Parameters for 7T SRAM Cell in Nanometer Era," *2012 Second International Conference on Advanced Computing & Communication Technologies*, 2012.

[17] S. S. R., B. R. S., Samiksha, R. Banu, and P. Shubham, "Design and Performance Analysis of 6T SRAM Cell in 22nm CMOS and FINFET

Technology Nodes," 2017 International Conference on Recent Advances in Electronics and Communication Technology (ICRAECT), 2017.

[18] Seo, H., Dong-keun Song, Ju-ho Lee, Mohamed G. Ahmed, and Tae-Won Cho. "A study on the memristor-based non-volatile 4T static RAM cell." In International Technical Conference on Circuits/Systems, Computers and Communications. 2011.

[19] K. F. Sharif, R. Islam, S. N. Biswas, and V. Groza, "4 Transistor and 2 memristor based memory," 2017 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE), 2017.

[20] C. Premalatha, K. Sarika, and P. M. Kannan, "A comparative analysis of 6T, 7T, 8T and 9T SRAM cells in 90nm technology," 2015 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), 2015.