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A 10-bit 100MS/s Memristor Based Pipelined ADC in Digital CMOS Technology

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Abstract*—This article proposed a 10bit 100 MS/s memristor based pipelined ADC intoday's digital Complementary metal-oxide-semiconductors technology. Here in this context, a technique is proposed in low voltage for a two-stage Complementary metal -oxide-semiconductors operational amplifier with 45 nm technology. In this paper operational amplifier, the backup power utilization is very low, the driving capacity is high and it operates at low voltage so that the circuit operates at low power. Low voltage circuit techniques and a neat configuration are suitable for achieving high resolution in a low power supply. A memristor is applied to regulate the memristence of the recompense block of the projected op amp. In this op-amp, the memristor replaces the resistors. The analog-to-digital converter has a sampling resolution of 100 bits / s in 10 bits resolution, a power consumption of 53.07 mV, a leakage current of 26.6 mA, a leakage power of 18.66 mW, 38.21 mV leak voltage, 22.9 db noise ADC will help reduce system-on-chip power consumption for digital consumer products and wireless communication products.*

1. INTRODUCTION

Op amp are today one of the magnificent consumed electronic tool sand are used in a wide range of user, manufacturing and technical devices. In many claims of op amp, the amplification of a single stage op amp is not enough. They use more than one gain stages [3] which are broadly used when developed profits are looked-for. This entails the summary of the further stage change, and compensation of these structures is necessary to uphold an adequate amplitude response or time response in the feedback loop using multi-stage architectures. In many topologies Operational amplifiers are available. The two-stage operational amplifier is another of a kind. They used it at ZL and at low ZS when they are needed.

I. Two stage Complementary Metal-Oxide-Semiconductors OpAmp layout.

The two stage OpAmp Complementary metal-oxide-semiconductors is depicted in Figure 1 composed of three sections:

- The input of differential stages,
- The second gain stages and
- The output of the buffer stages

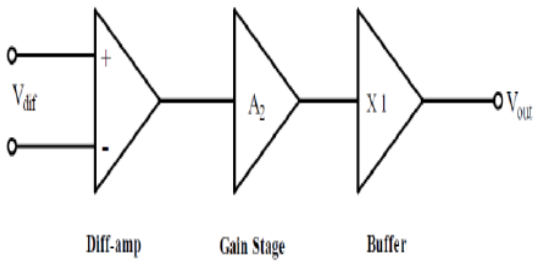

Figure 1. Block Diagram of Basic Two Stage Operational Amplifier

In the Illustration of conventional Complementary metal-oxide-semiconductors op amp of two stage is shown in the figure. The schematic design of the conventional two stage Complementary metal-oxide-semiconductors operational amplifier described in Figure 2. In this, the transistors are in pair M1and M2, M3 and M4 constitute in the 1st stage of the operational amplifier that is a differential amp. They total DC gain in the circuit was calculated on the output resistance of NMOS and PMOS.

CMOS op amp can be effectively used for practical values, such as the design of a switched capacitor filter, ADC [4], etc. fig1 shows the configuration of a Complementary metal-oxide-semiconductors operational amplifier of two stage. M5 provides polarization for the entire operational amplifier. Differential stage formed by the two pairs, M1 transistor and M2transistor, input the first stage of the operational amplifier. M5 and M7 supply a differential current pair IB1. M3 and M4 create the input current mirror. Then output of first stage of the operational amplifier was created by node 1. The second stage having two transistors M6 and M7, M6 is actively loaded by the transistor M7 which is a common source amplifier.

The second gain stage runs the current load followed by the first input stages. Normally, the final stage can be added to evacuate heavy loads from the chip but it is not used as such [3, 5]. In this section various parameters of performance of the CMOS operational amplifier circuit will be analysed.

Open circuit voltage gain, input resistance, output resistance cane shown in the PMOS a pair of differential channels consist in the first stage with a mirror charge of the channel NMOS and M5 is the source of the channel end current. This is the M7 current-channel load and the n-channel common M6 source amplifier and with that consist in the 2nd stage. Gates are connected to the inputs in the operational amplifier.

The resistance is the input most important when it comes to the MOS transistor. when the operational amplifier is used, in interior requests that do not require safety diodes, and then the operational amplifier is used.

An out resistor is a resistance that returns to the part of the inputs of an operational amplifier connected to a low signal mass:

$$Ro=r_{06}\|r_{07} \quad (1)$$

Although this output resistance is almost always much greater than that of commonly used bipolar operational amplifiers, low output resistance is generally not required for purely the load capacitor. The two stages can be considered separately in the diagram for the gain of voltage in the amplifier because the input resistance is infinite in the second stage.

That is considered as the precisely the same configuration in the first stage. The small is

$$A_{v1}=\frac{v01}{vi}=Gm1\ R_{01} \quad (2)$$

Trans conductance G_{m1} and
Output resistance is R_{01}

$$A_{v1}=g_{m1}\ (r_{02}\|r_{04}) \quad (3)$$

The second stage voltage gain

$$A_{v2}=-g_{m6}R_0 \quad (4)$$

The overall gain of the amplifier is

$$A_v=A_{v1}A_{v2}=-g_{m1}\ (r_{02}\|r_{04})\ gm_6\ (r_{06}\|r_{07}) \quad (5)$$

$$G_mr=\frac{2\ VA}{V0v} \quad (6)$$

The strong function can be considered by the initial voltage of the full voltage gain (proportional to the effective length of the channel) and saturation (defined as a function of the polarization conditions).

2. DESIGN WORKING

To describe the working of the op amp below given are some important relationship. Now we will proceed with the designing part

Slew rate, $SR = \frac{Is}{Cc}$ (1)

First-stage gain,

$$Av_1 = \frac{-gm}{gds^{2+}gds4} = \frac{-2gm_1}{Is(\lambda_2 + \lambda_4)} \quad (2)$$

Second-stage gain, (3)

Gain bandwidth, $GB = \frac{gm_1}{CL}$ (4)

Output pole, $P_2 = \frac{-gm_1}{CL}$ (5)

RHP zero, $z_1 = \frac{gm_6}{Cc}$ (6)

$$V_{in}\,(max) = VDD - \sqrt{\frac{Is}{Bs}} - [VT3\,(max) + VT1\,(min)] \quad (7)$$

$$V_{in}\,(min) = VSS - \sqrt{\frac{Is}{B1}} + VT1\,(max) + VDS5\,(sat) \quad (8)$$

$$VDS\,(sat) = \sqrt{\frac{2IDs}{B}} \quad (9)$$

Here all the transistors are in saturation it was assumed by the below given equation

$$g_{m1} = g_{m2} = g_{mI},\ g_{m6} = g_{mII},\ g_{ds2} + g_{ds4} = G\ I \text{ and } g_{ds6} + g_{ds7} = G\ II \quad (10)$$

1. This is the smallest selected device length has been selected to preserve the channel modulation parameter and ensure a good fit to the current mirrors.

2. Here the minimum value for Cc is selected in the desired phase margin, i.e. for a range of 600 phases. We used the some of the relationship. That is assumed by the with gain.

20GB.

Cc > 0.22 CL

In an operational amplifier layout, bipolar transistors offer many advantages over their Complementary metal-oxide-semiconductors counterparts, such as higher gain(gmr0)and higher trans conductance for a given current, higher speed, compensation voltage as a result, operational amplifiers consisting of bipolar transistors provide the best performance in many cases, including, for example, DC-coupled, low-deflection, and low-power applications. deflection. For these reasons, bipolar operational amplifiers have gained commercial importance while offering superior analog performance. However, Complementary metal-oxide-semiconductors technologies have become dominant in the construction of the digital parts of signal processing systems c, as they will change.

For an operational amplifier to have the largest swing possible, we must use this structure at the output of the operational amplifier. (Sometimes this output structure is called a push-pull amplifier because it can generate [push] and absorb [pull] a load current). The standard size is also changed in this structure. Then the final unit of the opamp and is to increase the input capacitor in the final process it was intended to increase the both. This capacity will be used to compensate the operational amplifier. Aol, is still large, the usage of the gain out stage rises A01 in the operational amplifier in addition with the operational amplifiers open switched gain.

This design, we used a capacitor for the output stage that lowers the dominant pole and stabilizes the operational amplifier. When the tuning time of the operational amplifier unfortunately increases, while 70MHZ is frequency of the op amp in the unit gain.

Although reduction in the capacitive load decreases setup time, we may not have options furthermore.

The charge is purely capacitive. We can consider eliminating the floating power source and the push-pull output stage. While the output range is reduced when the push-pull output buffer is not used, stability is almost guaranteed with a reasonable size load capacity. The bias current is increased in order to drive the capacitive load in the required time. An increase in scale of bias currents is followed by an increase in the size of the devices. For example, if we increase

our nominal polarization current from 15 µA to 150 µA, the size of our NMOS increases slightly and the size of the PMOS is very high.

The circuit we use in which the stabilization time is too long. By reducing the length of the push-pull output stage, we obtain the frequency of the second pole.

3. TWO STAGE CMOS OPAMP

The designed op_amp has been simulated to find several features of the proposed op_amp. The total project made in the cadence tool. Different test benches were created, then a project with parasitic values was separated and compared with the system. Subsequently, we compare the parameters of the device obtained by simulation with the device specification. The following is the conventional layout of the two-stage operational amplifier Figure 1. It affects the maximum capacity to load and unload the CL load.

The paper simulation results presented were obtained using 90 nm CMOS technology. After the simulation, to optimize the performance, it was necessary to change most of the sizes of transistors. The advantages of a two-stage operational amplifier are: good gain, high output power, low noise and good bandwidth. Currently, the operational amplifier project aims to achieve high amplification while optimizing the optimization of all process parameters.

The circuit designed to see the required conditions is described in Figure 1. The topology of this layout is the CMOS standard operational amplifier. This designed circuit of the CMOS operational amplifier comprises three subsections, namely the degree of differential gain, the second stage of amplification and the voltage chains. The main objective of this topology was to successfully complete all the design specifications. [one]. The layout is described below.

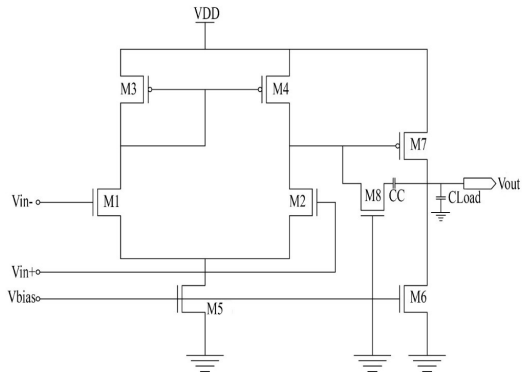

Figure 2: Conventional circuit of two stage op amp

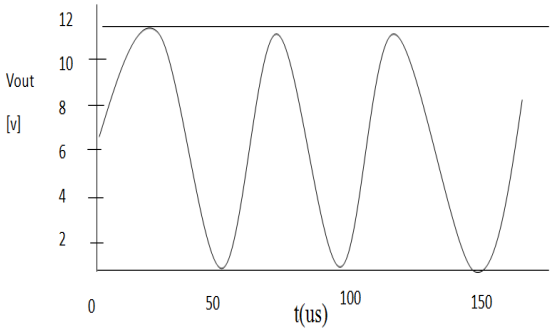

Figure 3: Waveform of the op amp

4. MEMRISTOR BASED OP AMP

The need to develop an operational amplifier capable of supporting a wide gain range on the chip is needed to develop futuristic neuron-based devices [3, 4]. Memristor, a memory connection, is basically the fourth missing element in two points of conventional electrical components that are capacitor, resistors and inductors. The nonlinear effects are exhibit by the memristor and it is a nanoscale element[21]. It contains both regime of action and initial resistance. The electrical resistance increases due to the current flowing in the memristor in one way [21]. Thus the electric resistance reduces when the current flowing in the opposite direction. In this event of a power failure, the memristor retains its last electrical resistance. Both properties of the memristor attracted the most attention. First, its dimensions at the nanoscale and, secondly, the characteristics of non-volatile memory.

$$Imem = I_R = \frac{Vsupp}{Vmem} = -\frac{Vout}{R1}$$

$$\frac{Vsupp}{Vmem} V \frac{Vout}{R1}_{out} = - \frac{R1}{Rmem} V_{supp}$$

In [2], the working of the circuit is divided between the two stages based on that memristor it is divided first is the programming stage and second is the main work stage.

In the programming stage, In the analog circuit the design specification are the cause of the changes in the values from initial value to another value in the memristor specification.

The memristor which are considered as the simple resistor are the programmed memristor in the main work stage. In the most common analog circuit the problem of compensation is one of the major challenges of operational amplifiers. To improve the bandwidth, frequency response and gain a precise adjustment of dominant poles and zeros is considered for compensation in analog circuits.

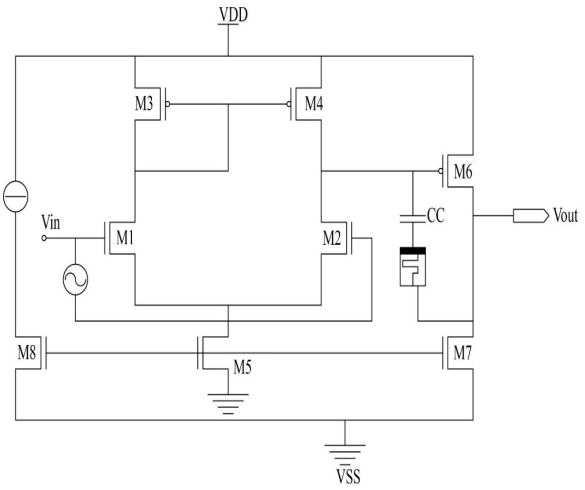

Figure 4: Memristor Based two stage op amp

In this op amp was developed for large scale simulation to describe computation and giving output [6] after giving attaching the memristor. With different ways of amplitudes memristor updated the process using a 1 second pulse. The starting time is large and the learning speed with the memory parts are a way too slow. However, the learning and training process is a unique process in the neural network. After training at the test stage, reading time is short and data processing is fast.

5. SIMULATION RESULTS

An experimental prototype of the ADC was manufactured in 90 nm Complementary metal-oxide-semiconductors technology. The total energy consumption is 10.01nW and samplerate of 100MS/s and supply1 V. The circuit shows compliance with the requirements given in the supposed conditions, that is, at room temp, supply of voltage of 1 V and typical values can be used by the transistor model. It described the measured non-linearity of the performance of Analog Digital Converter with a precision of 10 bits at 100 MS / s. In this leakage current it is 13.89PA and the leakage power is 9.08Pw due to the memristor shown in Table 1. A capacitor is connected to it.

In addition to these simulations performed with the operational amplifier in non-switching arrangement, the stable simulation is done under rare case. The operational amplifier is linked in a single reaction in the closed loop arrangement in this simulation. The reason of the stability simulation is to showing the behaviour of the layout at that time loop closes or to clarify if it is possible for it to occur. Through some careful calculations and precautions were taken while designing this operational amplifier.

Table 1: Parameter Comparison

	Power Con-sumption	Leakage current	Leakage power
Conventional	53.07nW	26.66PA	18.23Pw
Memristor	10.01nW	13.89PA	9.08Pw

The presentation synopsis of ADC shown here below in this below Table on which that circuit is design to get the specified output. It précises the functioning of ADC at a sampling rate calculation of 100MS/s in 90 nm CMOS Process. Particularly the power

utilization is just 10nw at 1 V supply voltage. So, it is running at a comparable sampling rate. We indent to apply this ADC to the SoCs of the digital consumer products and wireless communication equipment.

Table 2. Performance Summary of ADC

Technology Process	90nm CMOS tech-nology
Resolution Bits	10 bits
Calculation of Sampling Rate	100MS/s
Supply of Voltage	1V
Total Power Consumption	10nW

Below given figure 5. Shows the comparisons between the conventional two stage operational amplifier and the memristor based two stage operational amplifier.

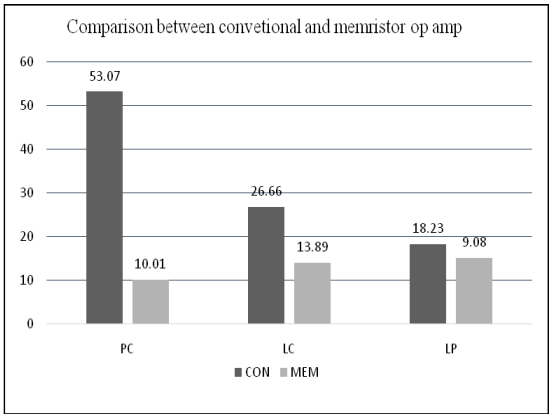

Figure 5. Comparison of conventional and memristor op amp

6. CONCLUSION

The main principal of this work was to implement the full specified sketch whose voltage is low and power is also low in this two-stage op amp with a memristor. There I a well specified method for the schematic of dualphase CMOS op amp has been presented. The plot has been made through the scaling factor to a minimum value can reduce current, power consumption and area as well. A memristor is used to reduce the power, maintain reliability, and resistency. So, it can store more information. The result of the simulation showed an improvement in the performance of the operational amplifier in terms of power, current, when implemented using memristor elements instead of capacitors and conventional resistors. The circuit diagram shown in this paper shows that using a sampling rate of usual CMOS processes can reach over 100 MS/s with parallel pipe architecture interspersed over time.

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